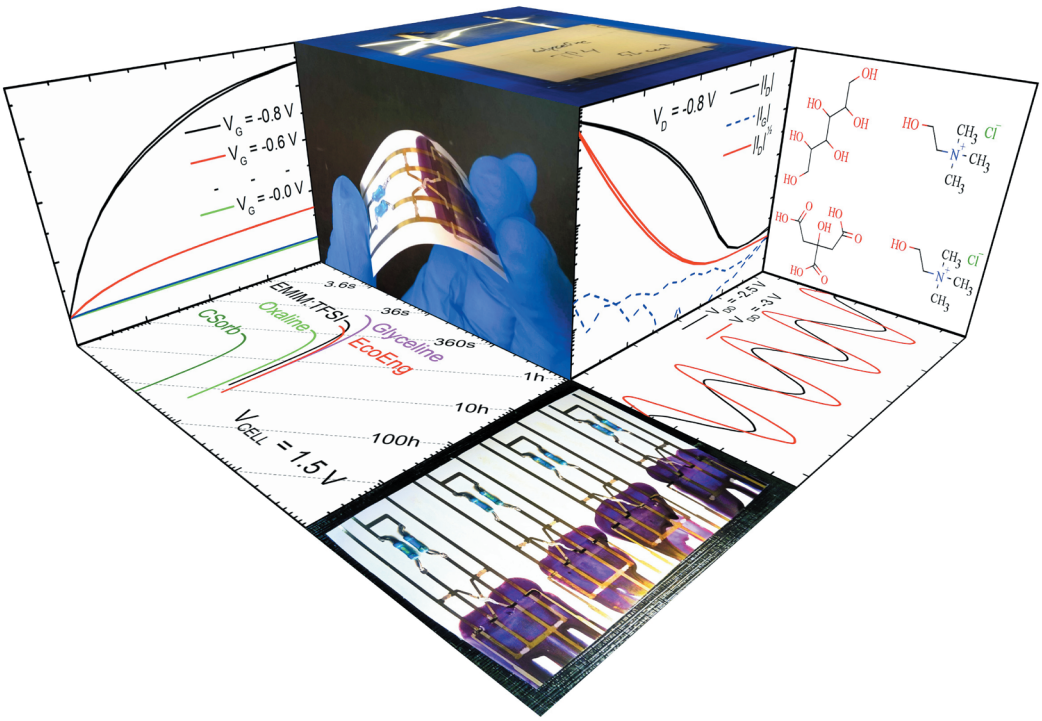
Åbo Akademi University

Fredrik Pettersson

Paper- and Membrane-Based Ion-Modulated Electronics



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Paper- and Membrane-Based Ion-Modulated Electronics

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Fredrik Pettersson

Contents

List of included publications

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IEEE Journal of the Electron Devices Society, **3**, 58 (2015)

Paper II. *Ion-Modulated Transistors on Paper using Phase-separated Semiconductor/Insulator Blends,*
F. Pettersson, R. Österbacka, J. Koskela, A. Kilpelä, T. Remonen, Y. Zhang, S. Inkinen, C.-E. Wilén, R. Bollström, M. Toivakka, A. Määttänen, P. Ihalainen and J. Peltonen,
MRS Communications, **4**, 51 (2014)

Paper III. *Environmentally Friendly Transistors and Circuits on Paper,*
F. Pettersson, T. Remonen, D. Adekanye, Y. Zhang, C.-E. Wilén and R. Österbacka,
ChemPhysChem, **16**, 1286-1294 (2015)

Paper IV. *Printed Environmentally Friendly Supercapacitors with Ionic Liquid Electrolytes on Paper,*
F. Pettersson, J. Keskinen, T. Remonen, L. von Hertzen, E. Jansson, K. Tappura, Y. Zhang, C.-E. Wilén and R. Österbacka,
Journal of Power Sources, **271**, 298 (2014)

Author's contribution

The work presented in this thesis is mainly based on experiments planned, performed and analyzed by the author. Some particular contributions to the different papers by the author are listed below:

Paper I. The author of this thesis did all the experimental work presented in this paper. Electrical expertise was provided by Janne Koskela and the membranes were provided by Carl-Johan Wikman. The manuscript was written by the author and was finalized together with the co-authors.

Paper II. The author of this thesis did all the experiments presented in the paper. The original idea of using phase-separation in our transistors is attributed to Daniel Tobjörk and further developed by the author in collaboration with Tommi Remonen and Yanxi Zhang. The manuscript was written by the author and finalized together with the co-authors.

Paper III. The author of this thesis did all the experiments presented in this paper except the logic gates presented at the end of the paper. They were done by David Adekanye under the supervision of the author. The deep eutectic mixture concept of electrolytes was developed by Tommi Remonen. The manuscript was written by the author and finalized together with the co-authors.

Paper IV. The author of this thesis did all the experimental work presented in this paper except fabrication of the AC electrodes and the confocal imaging. The electrodes were done by Jari Keskinen and Leo von Hertzen and the confocal imaging by Max Johansson. The manuscript was written by the author, Jari Keskinen and Tommi Remonen and finalized together with the co-authors.

List of other publications

Paper 1. *An Impedimetric Study of DNA Hybridization on Paper-Supported Inkjet-Printed Gold Electrodes,*
P. Ihalainen, F. Pettersson, M. Pesonen, T. Viitala, A. Määttänen, R. Österbacka and J. Peltonen, Nanotechnology, **25**, 094009 (2014)

Paper 2. *Impact of humidity on functionality of on-paper printed electronics,*
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Paper 3. *Cellulose-based ionogels for paper electronics,*
S. Thiemann, S. Sachnov, F. Pettersson, R. Bollström, R. Österbacka, P. Wasserscheid and J. Zaumseil, Advanced Functional Materials, **24**, 625 (2014)

Paper 4. *Origin of equilibrium charges in poly(3-hexylthiophene):[6,6] phenyl-C61-butyric acid methyl ester solar cell devices,*
M. Nyman, F. Pettersson and R. Österbacka, Chemical Physics, **404**, 60 (2012)

Paper 5. *Controlling the turn-on-voltage in low-voltage Al_2O_3 organic transistors with mixed self-assembled monolayers,*
N. Björklund, F. Pettersson, D. Tobjörk and R. Österbacka, Synthetic Metals, **161**, 743 (2011)

Paper 6. *Enhanced performance of printed organic diodes using a thin interfacial barrier layer,*
K. Lilja, H. Majumdar, F. Pettersson, R. Österbacka and T. Joutsenoja, ACS Applied Materials & Interfaces, **3**, **7** (2011)

Paper 7. *All-printed low-voltage organic transistors,*
D. Tobjörk, N. Kaihovirta, T. Mäkelä, F. Pettersson and R. Österbacka, Organic Electronics, **9**, 931 (2008)

List of patents

Patent 1. *Electroactive Blends and Layers, and Devices made from these*, WO 2015028700 A1, T. Remonen, F. Pettersson. R. Österbacka, Y. Zhang, D. Tobjörk, S. Inkinen and C.-E. Wilén

1. Introduction

This chapter introduces the general fields of the transistor and its application in logic circuits followed by energy storage devises. In Section 1.2, the organic field-effect transistor as well as the different models of organic ion-modulated transistors (IMTs) used and the special methods developed to create paper transistors are described. In Section 1.3, the logic gates developed using paper- and membrane-based transistors are presented and finally in Section 1.4 the environmentally friendly supercapacitor (SuC) on paper is presented.

1.1. Background

1.1.1. Transistors and logic gates

A transistor [1,2] is a three terminal device that is used in electronic circuits to control a large signal between two of the transistor terminals by applying a small signal between two other terminals. As a small change in the input signal translates to a large change in the output signal, the transistor can be used as an amplifier. This is also known as gain. The most common transistor type used in modern digital and analog circuitry is the metal oxide semiconductor field-effect transistor (MOSFET). [3] It was invented in 1959 at Bell Labs and was used in the first microprocessors created. [4] In the early 1970s, p-type and n-type MOSFETs (PMOS and NMOS, respectively) were used separately in microprocessors. Later on they were combined to create complementary-MOS (CMOS) technology. [5] The advantage with CMOS is that it has low power consumption and is not prone to overheating, e.g. when compared to NMOS- or PMOS-only electronics. [6] This sparked the interest in these types of field-effect transistors and much effort was put into researching and developing them further and with the development of clean rooms etc. smaller and more efficient transistors were made. This eventually led to the world's first mass-produced, truly portable, personal computer at the beginning of the 1980s. This intensive research also led to other types of transistors being developed, for this thesis the most important being the organic field-effect transistor (OFET), demonstrated by Tsumura et. al. [7] in 1986, as one of the first of its kind and immediately after that, in Finland, a similar OFET was demonstrated by Kuivalainen et. al. [8] The main reasons for developing the OFET has been environmental, economic as well as the fact that organic semiconductors can be solution-processable and large-area fabrication processes can be utilized without expensive clean rooms. [9,10] Another advantage is that organic semiconductors can be flexible and, thus, roll-to-roll (R2R)-compatible fabrication

processes can be used to create cheap transistors on many substrates not suitable e.g. for silicon-based electronics. [11–13] Flexible substrates such as PET, paper and even textile fibers have been used to fabricate transistors on. [14] This opens up possibilities to create all imaginable sorts of applications, such as sensors and displays printed directly on food packages and shipping boxes, battery charging and health monitoring devices incorporated into the textile of clothing, bendable displays for wrist watches, solar cells painted directly onto roofs, light emitting paint on walls etc. Organic based electronics is also used when interfacing with live tissue [15,16] and has even been shown to outperform inorganic electronics in that area. [17]

In this thesis, methods to create transistors on rough and absorptive substrates are being investigated, as well as making the devices more environmentally friendly and also, improving the switching speeds of the devices. Each of the methods presented to solve these issues are usually accompanied by some other form of decrease in performance. The trick is to evaluate the trade-offs and try to find an optimized solution that makes the device as good as possible within the set parameters.

1.1.2. Energy storage units

The Volta cell was invented in the 1800s and consisted of zinc and copper electrodes separated by cardboard and used brine as the electrolyte. [18] During operation, the cell utilizes electrochemically stored energy so that the zinc is being oxidized and releases ions into the electrolyte, leaving electrons in the metal that join with hydrogen ions in the electrolyte through an external connection to the copper electrode, creating hydrogen gas. As the zinc is being dissolved into the electrolyte, the cell is non-rechargeable. The present day cell was invented in 1949 and consisted of zinc and manganese electrodes and used alkaline electrolytes. The rechargeable battery was invented in 1859 (lead-acid) [19] and further improvements were made over the following years. The Li-ion battery, used in most electronic gadgets today, was invented in 1977. [20] The electric double layer capacitor (EDLC), invented in 1957 by H.I. Becker [21] and also the type of energy storage unit presented in this thesis, is both rechargeable and non-Faradaic. In the EDLC, which consists of two metal electrodes separated by a separator and electrolyte, the charges are stored electrostatically on the surface of the electrodes and no charge is being exchanged between the electrodes and electrolyte. The electrolytes and electrodes were further improved over the years but the same principal device is still used today in most EDLCs. Since the device structure is fairly simple, the electrodes can be made with carbon and the electrolyte can be almost any sort of ion-conducting material. The EDLC model is a superb

alternative for developing environmentally friendly energy storage devices, since the fabrication processes are roll-to-roll compatible and the materials used can be cheap and environmentally friendly. Supercapacitor is the term that will be used in this thesis when describing these types of devices. The term is a product name of the Nippon Electronic Company presented in 1971 [22] referring to the large area of the electrode materials used, in this case activated carbon-covered aluminum electrodes as well as the extremely high capacitances that are achievable when utilizing EDLs. The abbreviation SuC will be used for the term supercapacitor so not to confuse the reader with the abbreviation for the term semiconductor.

1.2. Transistors

This section on transistors is divided into two parts; the first one describing the OFET and how to characterize it and in the second one, the ion-modulated transistor, the transistor model used in this thesis, is presented in more detail.

1.2.1. Organic Field-Effect Transistors

The organic field-effect transistor (OFET) [7,23–28] structure is based on the thin film transistor (TFT) structure introduced by Weimer in 1962, [29] where all the layers of the device are thin and have been deposited, in some fashion, onto an insulating substrate. The main difference is that the OFET incorporates an organic semiconductor as opposed to an inorganic one that the presented TFTs used. The different parts of an OFET are the source- and drain electrodes, the semiconductor layer, the gate insulator layer and the gate electrode. These can be applied in different orders to create different transistor structures. It is important that the gate is separated from the semiconductor (and source- and drain electrodes) by the gate insulator and that the semiconductor is in contact with the source- and drain electrodes. An example transistor structure is drawn in Figure 1.1. The bottom-gate, top-contact structure has the gate on the bottom, separated from the semiconductor by the insulator, and the source and drain electrodes on top. If the gate is un-biased and a potential is applied over the source and drain, no current will flow through the device as the semiconductor is non-conductive in this state. If a negative potential is applied to the gate (p-channel), the insulator will become polarized and charges will be injected into the semiconductor, from the source, in order to compensate for the resulting electric field. The injected, positive, charges will move to the semiconductor/insulator interface creating the transistor channel. Charges can now flow between the source and the drain and the transistor is said to be in the on-state. This electric field induced charge injection gives the organic *field-effect* transistor its name.

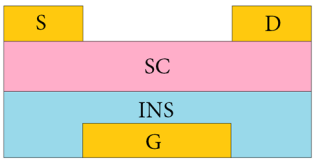


Figure 1.1. Top-contact bottom-gate configuration of an organic transistor. Source (S), drain (D) and gate (G) electrodes are colored in gold while the semiconductor (SC) and insulator (INS) are colored in pink and blue, respectively.

The OFET can be structured in many different ways and the materials can be applied in room temperature using a variety of techniques. [12] This makes it an appealing alternative to traditional silicon-based transistors. There are, however, some dimensional considerations that must be taken into account when fabricating OFETs. The channel length, e.g., should be minimized in order to maximize the current throughput. This can, however, be difficult to do using R2R-compatible fabrication techniques. The electrode overlap [30–32] is another issue that needs to be considered as stray capacitances cause decreased device performance, both in the form of speed and gate-leakage. The individual layers should also be as thin as possible, without causing short circuits, in order to increase the electric field strength and device switching speeds. [33–35]

Even though the mechanism for charge transport in OFETs differ from that of traditional MOSFETs, the electrical response from the devices are similar and the traditional MOSFET equations can therefore be used to describe and characterize OFETs. The standard MOSFET Equations 1.1 – 1.5 below are taken from S. M. Sze´s "Semiconductor Devices". [36] The same equations are also used to characterize IMTs, even though they differ even more in operation than OFETs do from MOSFETs. A typical way to characterize an OFET is to apply a constant voltage between the source- and drain electrodes, vary the gate voltage and measure the source-drain current, I_{DS}. This resulting *transfer* curve (see Figure 1.2 (a)) can then be used to determine a wide range of critical transistor values. An *output* curve, on the other hand, is measured by varying the source-drain voltage, V_{DS}, and measuring I_{DS}. Different *constant* gate voltages, V_G, are applied during these measurements and several traces of I_{DS}, at different V_G, are plotted as a function of V_{DS} (see Figure 1.2 (b)). The output curve can be used to determine when the transistor operates in the *linear* regime and when it operates in the *saturated* regime. When I_{DS} increases linearly with V_{DS}, the transistor is said to be operating in the linear regime. When I_{DS} stops increasing with increasing V_{DS} and saturates, the transistor is said to be operating in the saturated regime. The two regimes are marked in Figure 1.2 (b). In the linear regime ($V_{DS} << V_G$) the current

flow between the source and drain is not limited by the charge concentration in the channel and the current has an ohmic behavior. I_{DS} can be expressed as:

$$I_{DS}^{lin} = \frac{W}{L}\mu C_i \left(V_G - V_T - \frac{V_{DS}}{2}\right) V_{DS} \qquad (1.1)$$

where W and L are the channel widths and lengths, respectively, μ is the field-effect mobility of the charges in the channel, C_i is the insulator capacitance and V_T is the threshold voltage. In the saturated regime ($V_{DS} > V_G$) the current flow becomes limited by the charge concentration in the channel and the current remains constant even if V_{DS} increases. This saturated current is then expressed by using Equation 1.1 and setting $V_{DS} = V_G$:

$$I_{DS}^{sat} = \frac{W}{2L}\mu C_i (V_G - V_T)^2 \qquad (1.2)$$

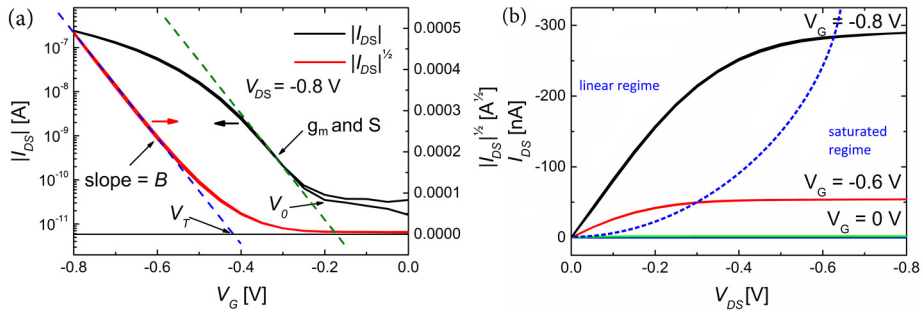


Figure 1.2. Typical (a) transfer- and (b) output curves of OFETs. Usually, the absolute drain/source-current ($|I_{DS}|$) is shown on a logarithmic scale (black curve) while the square root of the same current ($|I_{DS}|^{½}$) is shown on a linear scale (red curve) in the same graph. The gate current (not shown) is also typically drawn in the same graph on a logarithmic scale. The blue dashed line (B) is an extension of I_{DS} in the saturated regime. The threshold voltage (V_T) is determined by using the intersection of B and the V_G-axis. The green dashed line is used to determine the transconductance (g_m) and subthreshold swing (S).The output curve usually shows I_{DS} as a function of the drain/source-voltage (V_{DS}) for different gate voltages (V_G). The linear- and saturated regimes are separated by the blue dashed line.

The transfer curve is used to determine several critical transistor values and it can be measured both in the linear- and in the saturated regime. Note that only a transfer curve measured in the *saturated regime* is plotted in Figure 1.2. (a). The black curve is $|I_{DS}|$ vs. V_G plotted on a log/lin scale while the red curve is the root of the same data, i.e. $|I_{DS}|^{½}$ vs. V_G plotted on a lin/lin scale. Most of the critical transistor values can then be determined using Equations 1.1 and 1.2.

The threshold voltage (V_T) is the minimum gate voltage needed to create a conduction path between source- and drain electrodes. Traps at the semiconductor/insulator interface are usually the source of $V_T \neq 0$ V that is often observed. These traps need to be filled before the conduction channel can be opened, i.e. resulting in a $V_T \neq 0$ V. The transfer curve is also used to extract V_T. In the linear region, when I_{DS} is plotted as a function of V_G, V_T can be found by extrapolating the curve slope, B, and determining its intersection with the V_G-axis. The same can be done for a transfer curve measured in the saturated region. However, since I_{DS}^{sat} has a square dependence on the gate voltage (see Equation 1.2), the square root of I_{DS}^{sat} should be plotted versus V_G. The same method can then be applied as in the linear regime to determine V_T. The threshold voltage has been determined using this method and is marked in the transfer curve (saturated regime) plotted in Figure 1.2 (a). The turn-on voltage, V_0, is defined as the V_G at which I_{DS} starts to increase exponentially. The physical origin of V_0 is very similar to V_T and a change in one is usually followed by a change in the other. The transistor off-current, I_{OFF}, which usually is a result of unintentionally doped semiconductor, is extracted at V_0 (see Figure 1.2 (a)). Another important value that is extracted from the transfer curve is the transconductance, g_m, or simply put, the transistor gain. It is the ratio between the change in output and the change in input. By using Equations 1.1 and 1.2 g_m is defined as follows, in the linear and saturated regime, respectively:

$$g_m^{lin} = \frac{\partial I_{DS}^{lin}}{\partial V_G} = \frac{W}{L}\mu C_i V_{DS} \qquad (1.3)$$

and

$$g_m^{sat} = \frac{\partial I_{DS}^{sat}}{\partial V_G} = \frac{W}{L}\mu C_i (V_G - V_T) \qquad (1.4)$$

The point on the transfer curve where the slope is the steepest is used to determine g_m. It then follows that the mobility (μ) is easily extracted using Equations 1.3 and 1.4. It can also be directly extracted from the transfer curve, measured in the saturated regime, by using the slope of the extrapolated line, B, (also used to determine V_T, above) where $\sqrt{I_{DS}^{sat}}$ was plotted as a function of V_G. The mobility is then determined as:

$$\mu = \frac{2LB^2}{WC_i} \qquad (1.5)$$

It should be noted that μ is assumed to be constant at all V_G in these equations. This is, however, not true for OFETs since, according to the extended Gaussian disorder model for transport in disordered semiconductors, the mobility is dependent on temperature, field and charge carrier density. [37–40] Especially in the IMTs presented in this thesis where ions penetrate the semiconductor, the mobility variations can be even more prominent.

The next thing that can be extracted from the transfer curve is the subthreshold swing, *S*. It describes how sharply the device turns from off-state to on-state and is given in units of [V/dec]. It is extracted at the same point as g_m and describes how much change in V_G is required in order to increase I_{DS} by one magnitude. Another property that can be determined from the transfer curve is e.g. the speed of the device. This can be done by scanning the transfer curve in both directions and drawing both I_{DS} curves on top of each other. Hysteresis indicates that the device is slow to switch between off-state and on-state, if the measured current is smaller in the forward sweep compared to the backward sweep. [35,41] This is especially typical for electrolyte gated- and electrochemical transistors, where the relaxation of ion-motion, during operation, can be slow. Hysteresis in the other direction can e.g. indicate some form of reversible or irreversible degradation of the device. [42] Other values that can be extracted from transfer curves are gate-leakage, on-currents, on/off-ratios, etc.

The methods of characterizing transistors presented above are used to characterize the IMTs presented in this thesis, even though the operating mechanism of the IMTs is clearly different than that of the classical MOSFET devices the equations were constructed for. It is, however, a good approximation and it is also common practice in the field of IMTs to do so.

1.2.2. Ion-Modulated Transistors

In field-effect transistors, when the gate is being biased, the dielectric layer becomes polarized (the electron distribution, in the bonds between the atoms, re-arranges) and the channel in the semiconductor is formed via the field-effect. The gate-dielectric-channel system, plotted in Figure 1.3 (a), can be viewed, in an equivalent circuit, as a parallel plate capacitor where the gate and channel represent the plates and the dielectric the insulator of the capacitor. When the plates are charged the dielectric is polarized (Figure 1.3 (a)) and the capacitance, *C*, can be calculated using Equation 1.6.

$$C = \frac{k\varepsilon_0 A}{d} \tag{1.6}$$

Here, k is the relative permittivity of the dielectric, ε_0 is the permittivity in vacuum, A is the area of the plates and d the distance between the plates.

The situation is critically different in an IMT, where the dielectric layer is replaced with an ion-conductor (Figure 1.3 (b)). [43] All transistor types that have the channel modulated by ions fall under the description of IMTs. [14,35,44–46] Terms such as electrolyte-gated transistors (EGTs), electric double layer transistors (EDLTs) and ion-sensitive field-effect transistors (ISFETs) have also been used to define such devices. In this thesis, when talking about transistors, the term *ion-conductor* (ICon) will be used to define the material in the physical space between the gate and the semiconductor in all the IMTs, in the same way as e.g. the term dielectric is used in a classical TFT. In the ICon in the IMTs, the ions are mobile and the equivalent parallel plate capacitor operation changes drastically. During IMT operation two half-reactions occur at the ICon interfaces according to the following description:

When the gate is negatively biased compared to the source and drain electrodes, the first half-reaction entails positive ions (cations) in the ICon attracting to the gate surface creating an electric double layer (EDL), according to the Helmholtz model. [47–50] According to this simple model of the EDL, the gate electrode represents one capacitor plate while the cations attracted to the gate surface represent the other capacitor plate. In reality, the situation is more complicated as the arrangement of the ions at the surface in the ICon is more complicated than a single layer of ions neatly stacked at the surface. The Gouy-Chapman-Stern model [51] e.g. describes a thin inner layer of static ions and a thicker diffusive layer of ions that extend deep into the ICon. However, for the purpose of this discussion, the simple Helmholtz model for the EDL will suffice.

The second half-reaction occurs at the opposite ICon/semiconductor interface whereto the negative ions (anions) are repelled. In order to neutralize the electric field created by these anions, holes are injected into the semiconductor from the source and drain electrodes and a layer of holes is formed at the ICon/semiconductor interface. This layer of holes is also known as the transistor channel. The EDL at this interface then consists of the layer of anions and the layer of accumulated holes. The bulk of the ICon remains charge-neutral and the entire electric field created is dropped across the two EDLs formed at the individual interfaces. This situation, depicted in Figure 1.4 (b) can then be viewed as two parallel plate capacitors connected in series, with the gate and the cations as the plates of one capacitor, separated by a distance d_1, and the anions and holes as the plates of the other capacitor, separated by a distance d_2. The resistance of the ICon between the two capacitors is disregarded in this simplified explanation, since in steady state it does not contribute to the capacitance of the system. [52]

The individual capacitances C_1 and C_2 can thus be calculated using Equation 1.6, d_1 and d_2. The total capacitance, C_{TOT}, (Equation 1.8) can thus be calculated using Equations 1.6 and 1.7.

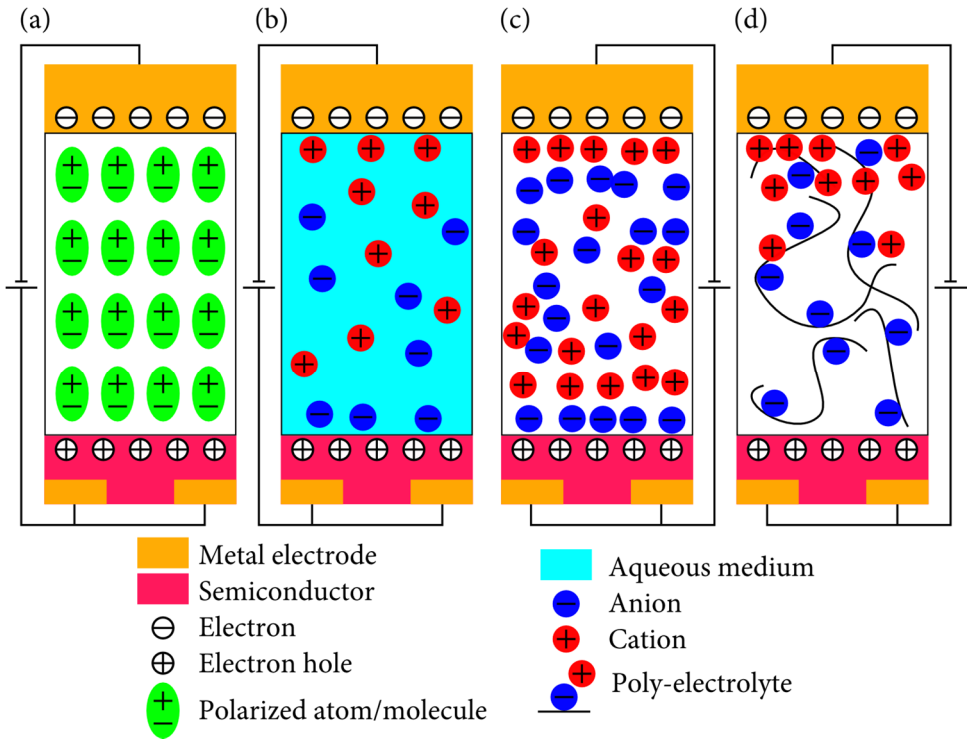


*Figure 1.3. A negative bias is applied on the gates of transistors with different dielectric/ICon layers. (a) The **dielectric** of an OFET is polarized and charges accumulate in the channel, (b) the mobile ions in an **electrolyte** form EDLs at the two interfaces, one of which includes the transistor channel, (c) the mobile ions in the **ionic liquid** (IL) form EDLs at the two interfaces, one of which includes the transistor channel and (d) the mobile cations move to the gate interface creating an EDL, leaving the bulk of the **poly-electrolyte** negatively charged with immobile anions and the transistor channel is formed. The bulk of the ICon in (b) and (c) remains charge-neutral.*

$$\frac{1}{C_{TOT}} = \frac{1}{C_1} + \frac{1}{C_2} \tag{1.7}$$

$$C_{TOT} = \frac{C_1 C_2}{C_1 + C_2} = \frac{k\varepsilon_0 A}{d_1 + d_2} \tag{1.8}$$

Comparing Equations 1.6 and 1.8 one can see that the only difference is that d is replaced with $d_1 + d_2$. The crucial difference is that d is the separation between the gate and the semiconductor while d_1 and d_2 are the separation between the ions

and holes (or electrons) in the EDLs. Fabricating field-effect driven transistors with small *d*:s on rough substrates can be difficult without creating pinholes, [53] whereas these potential driven transistors with EDL thicknesses (d_1 and d_2) less than one nanometer, [14] independent of the ICon layer thickness, are well suited for fabrication on rough substrates such as paper. Higher capacitances can thus be reached without creating ultra-thin ICon layers or by increasing the relative permittivity of the ICon.

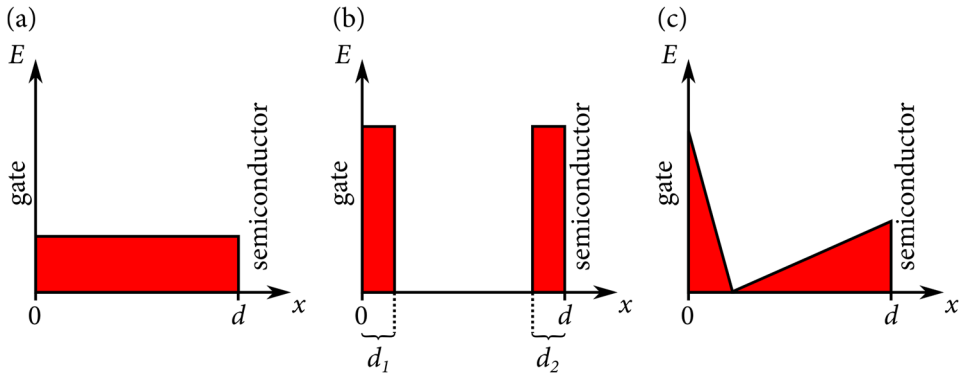


Figure 1.4. The electric field distribution, E, inside the dielectric/ICon layer of a) a traditional dielectric OFET, b) an IMT with electrolyte- or IL-like ICon, having mobile anions and cations, and c) an IMT with poly-electrolytic ICon, having only one mobile ion-species, when the gate is biased. The x-axis represents the gate-semiconductor direction, where 0 indicates the gate/dielectric (gate/ICon layer) interface and d the dielectric (ICon)/semiconductor interface and d_1 and d_2 the EDL thicknesses created at the individual interfaces, respectively.

Typical ICons used are electrolytes where free ion-species are mixed in a solution, usually water. Another, water-free, alternative that can be used as the ICon layer is ionic liquids (ILs). [54–56] In an IL there is no solution in which the ion-species reside. Instead, the ion-species form a sea of dissociated negatively- and positively-charged ions or associated charge-neutral ion-pairs. In short, ILs can be described as molten salts that melt at moderate temperatures. The capacitive properties of ILs, plotted in Figure 1.3 (c), are generally similar to that of electrolytes [57] and the electric field drops over the EDLs in a similar fashion as the one depicted in Figure 1.4 (b). A third option is a sort of mixture between a classical OFET dielectric and an IL, i.e. a poly-electrolyte, [45,58,59] plotted in Figure 1.3 (d). Here, one of the ion-species is attached to the backbone of a larger polymer network and is essentially immobile, while the counter-ion remains mobile. This results in a situation depicted in Figure 1.4 (c), where the electric field drop is distributed unevenly throughout the bulk of the ICon. This will result in a total capacitance somewhere in the middle of that of a classical OFET and that of an IL-type IMT. This setup can have several advantages, e.g. the polymer backbone can provide a

solid matrix for the counter-ion to move around in or the immobile ion can be prevented from penetrating the semiconductor and causing unwanted electrochemistry. This type of poly-electrolyte is used as ICon in the enhancement mode p-channel IMT (EM PIMT) presented in **Paper I**. The same poly-electrolyte is also used as a proton bridge (the term *ion-conductor* is again used to describe the material in the physical space between the gate and the channel) in the depletion mode p-channel IMT (DM PIMT) presented in the same paper. This transistor type has a redox-active PEDOT:PSS as the active layer and the two transistor types operate in very different ways.

The EM PIMT and the DM PIMT are both built around a self-supporting and insulating (poly(vinylidene fluoride) (PVDF)) membrane that has been functionalized to be ion-conductive poly(vinylidene fluoride) poly(styrene) sulfonic acid (PVDF:PSSA) in selective places. As a result, the membrane can serve as both substrate and ICon in the different transistor types, simultaneously. The EM PIMT is vertically stacked according to the structure illustrated in Figure 1.5 (a) – (c), while the DM PIMT is both vertically and laterally stacked according to Figure 1.6, but for clarity a two dimensional representation has been drawn in Figure 1.5 (d) – (f).

As the ICon of the membrane is here a poly-electrolyte, only one ion (the cation H^+ in this case) is mobile, while the anion is bonded to the polymer backbone and therefore immobile. In the EM PIMT the channel is non-conductive when the gate is un-biased (Figure 1.5 (a)). When the gate is negatively biased, the protons in the ICon migrate towards the gate, penetrate the electro-active PEDOT:PSS gate and electrochemically reduce it. The remaining immobile anions in the ICon create a negatively charged field that is compensated for by positively charged holes accumulating in the transistor channel (Figure 1.5(b)). The channel is highly conducting and no more charge is accumulating (Figure 1.5 (c)).

The DM PIMT, on the other hand, has a conductive channel when the gate is un-biased. The channel is here a stripe of PEDOT:PSS. It is connected ionically to the (also) PEDOT:PSS gate via the ICon (Figure 1.5 (d)). Applying a positive gate bias oxidizes the gate PEDOT:PSS, protons migrate through the ICon, penetrate and electrochemically reduce the PEDOT:PSS channel (Figure 1.5 (e)). This process of reducing the channel turns the transistor off. When there is no more ion-motion in the device, the device is fully turned off (Figure 1.5 (f)).

For all their advantages with high capacitances and low sensitivity to substrate roughness the IMTs are slow to switch between operational states compared to that of traditional dielectric OFETs. [60,61] This is due to the nature of the mobility of the charged ions in the ICon. When an external electric field is applied over the ICon, i.e. a gate bias is applied, ions migrate inside the ICon as a

response to the electric field and the EDLs are eventually formed at the individual interfaces. This process is the rate limiting factor that makes them slower than traditional dielectric OFETs.

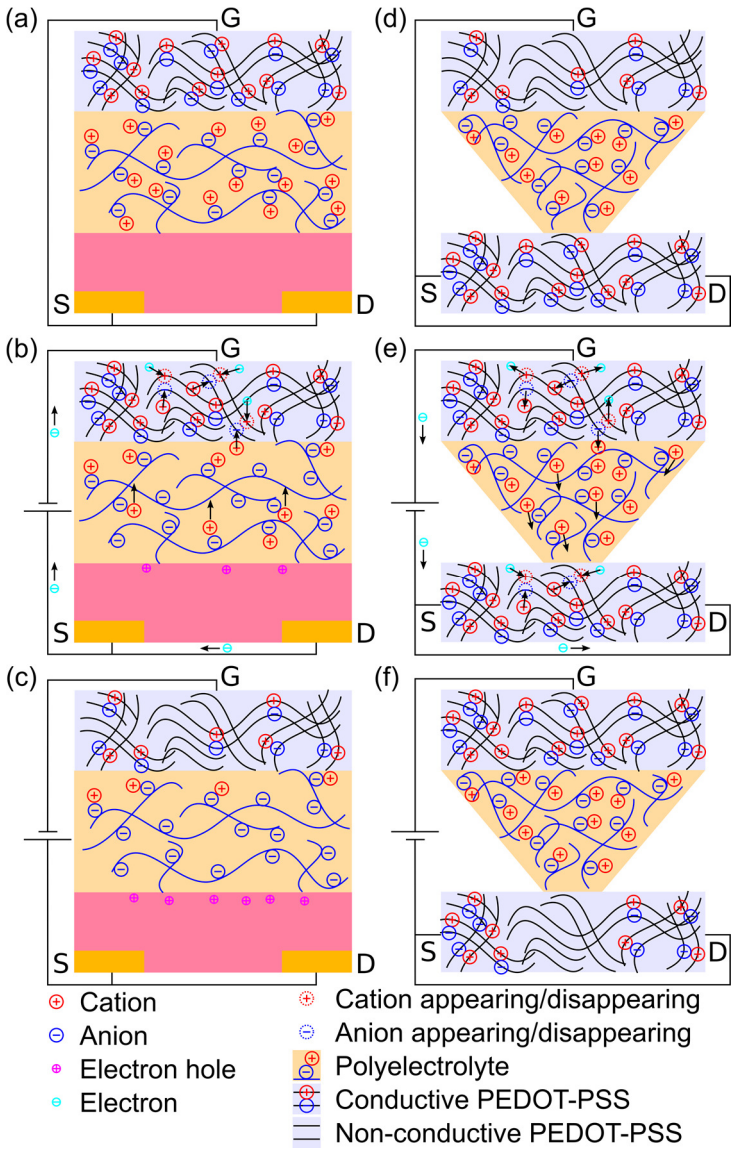


Figure 1.5. A schematic cross-section of an EM PIMT is depicted in (a), (b) and (c) and a DM PIMT in (d), (e) and (f). Light blue, yellow and pink areas indicate PEDOT:PSS, polyelectrolyte and P3HT, respectively and gold S- and D electrodes. The figures on top represent the devices in their natural un-biased states, the middle figures when the devices are being turned on and off, respectively and the bottom figures the devices in the on- and off-states, respectively.

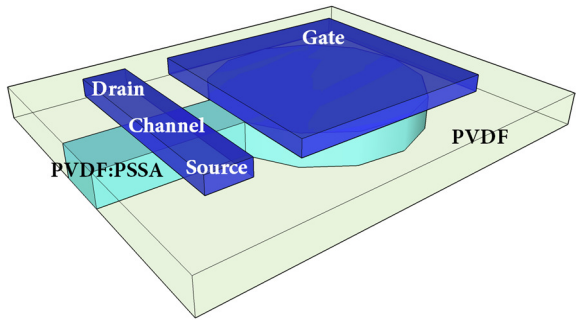


Figure 1.6. Device setup of the enhancement mode IMT. The white and light blue represents the patterned membrane containing both the insulating PVFD (white) and the ion-conducting PVDF:PSSA (light blue). The dark blue represents the drop casted PEDOT:PSS that make up the gate-, source- and drain electrodes and also the transistor channel.

A second and even more complicated process that can occur in IMTs with mobile ions is that the ions not only move to the ICon/semiconductor interface and create an EDL, but they can also penetrate the semiconductor and electrochemically dope it. [14] Further, the ions continue to move deeper into the semiconductor doping the entire bulk. This process of ion-migration inside the semiconductor is even slower than the ion-migration in the ICon discussed in the previous section. As the doped parts of the semiconductor are conducting and contribute to the source-drain current, high throughput currents are now achievable. This device can now be said to be electrochemical since the source-drain current flows through the bulk of the semiconductor, and not only at the ICon/semiconductor interface.

The time domains of the ion-migration in the ICon, the EDL formation and the last ion-migration in the semiconductor are strictly different and vary depending on the materials used; especially important are the internal resistance of the ICon and the ion-mobility in the semiconductor. This is one of the most important reasons why electrochemistry is unwanted in IMTs, and also why poly-electrolytes are used as the ICon layer in some transistors.

1.3. Logic Circuits

The next step that naturally follows after the basic electronic building blocks, such as transistors, have been created is building logic circuits. [62] In this chapter the focus will be on presenting simple inverters and continuing onto more complicated circuits, such as ring-oscillators, NOR-gates and finishing with memory devices, such as SR-latches.

1.3.1. Inverters

The inverter is a logic NOT-gate [63] that returns a state that is opposite to the input state, i.e. if the input is *true* the output will be *false* and vice versa. An inverter can be built using one, two, three or even more transistors, but the simplest model incorporates just one transistor. This can be done with any type of transistor (n-channel, p-channel, etc.) combined with a resistor, as long as the transistor has good enough electrical characteristics so that the inverter output is larger than the input. This is a requirement since more than one inverter is needed in order to create logic, i.e. one inverter must be able to supply the next one with current without signal decay. The output signal must also have an off-state lower than the off-state of the input and an on-state higher than the input on-state (see Figure 1.7.) The signal would otherwise drift in one direction after each inverter-stage making the electronic device useless. The basic inverter has four terminals: ground, supply voltage, input and output. The first two are typically constant while the latter two usually vary with time. A single-transistor (p-channel) inverter can be seen as inset in Figure 1.7.

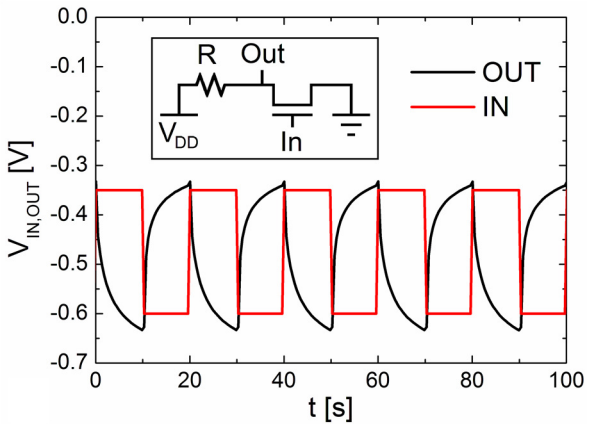


Figure 1.7. An example of the input- (red curve) and output voltages (black curve) of an inverter. It is important that the lowest output voltage is lower than the lowest input voltage and the highest output voltage is higher than the highest input voltage. The inset shows the connection diagram of the inverter.

Depending on the voltage applied to the transistor gate (inverter input) the transistor channel resistance (R_{SD}) will either be high ($R_{SD,ON}$) or low ($R_{SD,OFF}$). R_{SD} refers to the resistance between source and drain. The inverter resistor (R) must be chosen so that its value lies between $R_{SD,ON}$ and $R_{SD,OFF}$ in order for the inverter to work. A high (absolute) voltage applied to the input will make the channel highly conductive and all current will flow between ground and the inverter output, since

$R > R_{SD,ON}$. When a low (absolute) voltage is applied to the input, the transistor channel will be highly resistive, $R < R_{SD,OFF}$, and all current will flow between the supply voltage, V_{DD}, and the inverter output. It is now very important to have good transistor characteristics. For example, a poor on/off-ratio will make the different resistance values (R, $R_{SD,ON}$ and $R_{SD,OFF}$) too close to each other and result in some current flowing through the transistor, when all current should be flowing through the resistor and vice versa.

To alleviate some of these effects another transistor can be incorporated into the inverter replacing the static resistor. The new transistor must now be an n-channel device in order for the replacement to be useful. This type of setup is called a complementary-symmetry metal-oxide-semiconductor (CMOS) technology. [62–66] The advantage here is that the current will always be flowing through either of the transistors, never through both at the same time (only during switching). For the single-transistor inverter some current was always flowing from the supply voltage directly to the ground, creating excess heat. The CMOS inverter also switches faster than the single-transistor inverter. These are some of the reasons why CMOS technology has become so widely used, especially in integrated circuitry. The performance of the transistors used will dictate how well the inverters will operate. The most critical properties are the power consumption and switching speed. These depend directly and most importantly on the transistor gate-leakage, on/off-ratio and sub-threshold swing. The different inverter types used will be presented in **Papers I**, **II** and **III**.

1.3.2. Ring-Oscillators

The ring-oscillator is a row of inverters connected in series and the output of this series is fed back to the input of the ring-oscillator creating an endless loop of inverters (see inset of Figure 1.8.). [62–65] In order to achieve an oscillation an uneven number of inverters must be present in the loop, otherwise the device would constantly be in a stable state. In a loop of an odd number of inverters every inverter will constantly be switching the input of the next one. The switching speed will be a function of the gate-delay of each individual inverter-transistor. The gate-delay is defined as the time it takes to switch one transistor from off-state to on-state and vice versa. The frequency of the oscillation of the output of the ring-oscillator gives the propagation delay time of the oscillator according to Equation 1.9:

$$P = 2Nt_p \tag{1.9}$$

where P is the oscillation period, N is the number of inverters in the oscillator and t_p is the propagation delay time per inverter-stage. The last one (t_p) can be described as the phase-shift between the input and output of one individual inverter. A typical output of a ring-oscillator can be seen in Figure 1.8. The ring-oscillator setup is a useful demonstrator when developing new transistor types. There are several factors that need to be fulfilled for the ring-oscillator to function properly. Firstly, the individual inverters must amplify and invert the input signal. They must have the input levels within the output levels according to the description in Section 1.3.1. Many functioning transistors must be fabricated at the same time and they must have similar properties for the oscillator to operate. A working ring-oscillator is a strong indicator of whether the new transistor model can be a useful electronic component or not. The oscillation frequency also gives important information about the switching speed of the transistor. Several different ring-oscillators are presented in this thesis in **Papers I**, **II** and **III**.

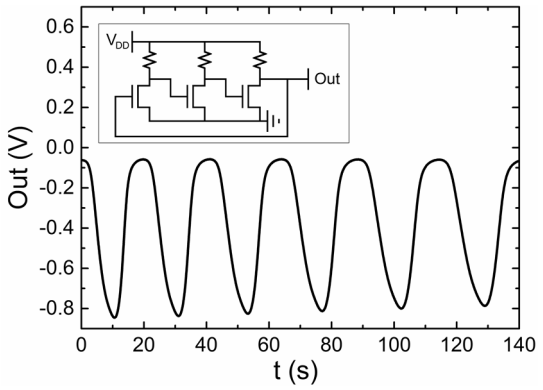
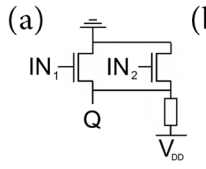


Figure 1.8. Typical output curve of a three-stage ring-oscillator with the connection diagram as inset.

1.3.3. NOR-Gates

The NOR-gate [62–66] is another example of basic logic gates that are required when building any type of electronics. To build one using OFETs at least two transistors are needed, when using n- or p-channel metal oxide semiconductor (NMOS or PMOS) technology only. The same advantages holds true for the NOR-gate as for the inverter when utilizing CMOS; faster switching and less power consuming devices can be built. When using CMOS usually four transistors are needed to create the NOR-gate. In this thesis, however, PMOS-only NOR-gates are created and in such a device two p-channel transistors and one resistor is required for the gate to function correctly. The device setup can be seen in Figure 1.9 (a).



(b)

IN_1	IN_2	Q
0	0	1
0	1	0
1	0	0
1	1	0

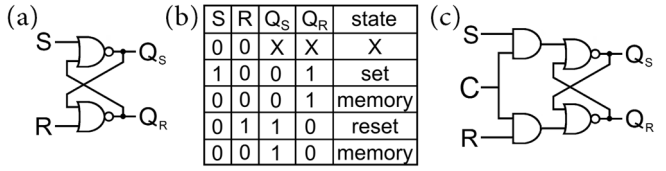
Figure 1.9. (a) The connection diagram of a NOR-gate constructed using two p-channel transistors and one resistor and the corresponding (b) truth table.

The two transistors are connected in parallel and the resistor, R, in series. The supply voltage, V_{DD}, is connected to R, the transistor drains are connected to the ground, the inputs IN_1 and IN_2 are connected to the transistor gates and the output Q is connected to the transistor sources. When the resistance of the transistor channels in off-state ($R_{SD,OFF}$) is higher than R and smaller in on-state ($R_{SD,ON}$), ($R_{SD,OFF} > R > R_{SD,ON}$), the current will flow between V_{DD} and Q only when both transistors are in off-state and between ground and Q in all other cases. The truth table for the NOR-gate is shown in Figure 1.9 (b). This NOR-gate set up may cause the two-transistor component to have three distinct resistance levels; R_1 when both transistors are turned on, R_2 when one or the other transistor is turned on and R_3 when both transistors are turned off ($R_1 < R_2 < R_3$). The closer R_1 is to R_2, the better. Otherwise the Q off-state will be split in two distinct voltage levels reducing the NOR-gate's usefulness. Also, if R_3 is too close to R_1 and R_2 the distinction between Q on- and off-state will be difficult.

These types of difficulties can arise if the characteristics of the transistor (on/off-ratio, sub-threshold swing, gate-leakage) are poor or marginal, which is typical when working with paper-based transistors. An environmentally friendly NOR-gate constructed on paper is presented in **Paper III**.

1.3.4. SR-Latches

The SR-latch [63,64,66] is one of the simplest forms of memory element that can be implemented using PMOS technology only. The function of the latch is to be able to retain one bit of memory. This operation requires, in this case, two sets of NOR-gates that have their outputs connected in a feedback loop according to Figure 1.10 (a). In this type of setup the outputs will depend not only on the current inputs but also on previous inputs, hence the memory effect. The truth table for this device can be seen in Figure 1.10 (b).



S	R	Q_S	Q_R	state
0	0	X	X	X
1	0	0	1	set
0	0	0	1	memory
0	1	1	0	reset
0	0	1	0	memory

Figure 1.10. (a) The connection diagram of an SR-latch. Two NOR-gates are connected to create the latch. (b) The truth table corresponding to the latch depicted in (a). (c) The connection diagram of a clocked SR-latch with two additional AND-gates.

The basic operation of the SR-latch is that two separate states (*set*, *S*, and *reset*, *R*) can be applied to the latch. The two states can be set by applying 1 and 0 or 0 and 1 to the *S* and *R* inputs. The memory effect comes from the fact that the state stored in the latch is retained even when 0 and 0 are applied on the inputs. The outputs of the SR-latch, Q_S and Q_R, are always each other's complements due to the latch setup, hence, $Q_S = Q_R$ is impossible, and even further, $S = R = 1$ is a forbidden state. The SR-latch is a transparent latch. This means that the output is immediately affected by a change at the inputs. This can be an unwanted feature, e.g. in shift registers, since several consecutive latches would see their states immediately propagated through the entire series, voiding the memory effect. This effect can be avoided by adding a separate clocking device to each SR-latch, e.g. by adding two AND-gates to the inputs of the latch, according to Figure 1.10 (c). This clocking, *C*, terminal allows for whatever state that is set to the *S* and *R* inputs not to propagate to the Q_S and Q_R outputs until *C* is set to 1. This feature makes the SR-latch, in this form sometimes called a clocked flip-flop, opaque and allows for the creation of e.g. shift registers. A shift register is a memory device that can be used to write, store and read a series of data bits on.

The SR-latch is a logic circuit that is fairly complicated to build, i.e. it contains many transistors, resistors and inter-connections. Being able to build such a complicated device using our transistors, is a feat that demonstrates that our transistors will also work in other, more complicated circuits. The same type of difficulties, stemming from poor gate-leakage, sub-threshold swing, on/off-ratio, are also associated with creating SR-latches as was described for the NOR-gate in the previous chapter. They are, however, magnified here since twice the number of transistors (each device introducing its own problems) are used here compared to the previous devices.

1.4. Supercapacitors

The supercapacitor (SuC) is an energy storage device constructed as a parallel plate capacitor. There are two major SuC types, namely electrostatic and electrochemical SuCs. [67,68] An additional third subgroup is the combination of the two above mentioned types. The names refer to the nature of the energy storing mechanism. In the SuCs presented in this thesis no electrochemistry occurs and these SuCs are therefore of the electrostatic kind. A SuC has the same principal physical shape and electrical characteristics as an ordinary parallel plate capacitor. The capacitance is, however, much larger than an ordinary capacitor. In the SuC the dielectric is replaced with an ion-conductor (ICon) in the same manner as was done for the IMT presented in Section 1.2.2. As a result of the EDLs a high capacitance is achievable in a SuC with sub-nanometer *d*s according to Equation 1.8. The situation has been drawn in Figure 1.11 (a) including the equivalent circuit and capacitance, again leaving out the ICon resistance, as was done in Section 1.2.2. In order to increase the capacitance, a situation depicted in Figure 1.11 (b) has be utilized. Here, the electrodes have been replaced with a porous, high surface area material (on the order of 1000 m^2/g). This will lead to further increase as Equation 1.8 still holds true and the surface area is increased.

The word 'super' in supercapacitor is partially used since the electrodes in such devices have an extremely high 3D surface area, e.g. AC or nanotubes, and partially due to the high capacitances that are associated with the electrostatic and/or electrochemical storage of charges on the individual capacitor plates. There are limits on how large surface areas can be created. Firstly, the size of the ions determines how small the pores can be made. One must take into account that in SuCs in general there can always be present a complex ordering of cations and anions in layered-, micelle- and/or other complex structures. [47–50,69,70] Secondly, the conductivity of the electrodes must remain high enough to carry charges from the outermost edges of the AC to the charge collectors. Otherwise, all unconnected electrode area will only create excess insulating layers that diminish the capacitance. Thirdly, the pathways to the electrodes must be large enough to facilitate the complex ion clusters to reach the electrode surface deeper in the electrode. Bottlenecks here will result in large internal resistances of the capacitor resulting in slow-chargeable devices.

The situation becomes more complicated when the electrode material is easily reducible or oxidizable. Then the ion can, even in aqueous ICon, reach the electrode surface and electrochemically oxidize it with electron charge-transfer. This Faradaic method of storing charge on the electrode is more efficient than the non-Faradaic EDL. This method of storing energy is sometimes referred

to as a pseudocapacitance. [68,71] Even though these energy storing methods (especially the Faradic kind) are similar to that of re-chargeable batteries they are both faster and can be charged and re-charged many more times (>100 000) when compared to the batteries. [71] The reason is that only electrostatic charge transfer between electrode and ICon can occur, while in the batteries both chemical and structural changes of electrochemical reactive materials occur when the electrochemically stored energy is being released. Repeated cycling eventually degrades the electrode materials, reducing the battery cycling capability to a few

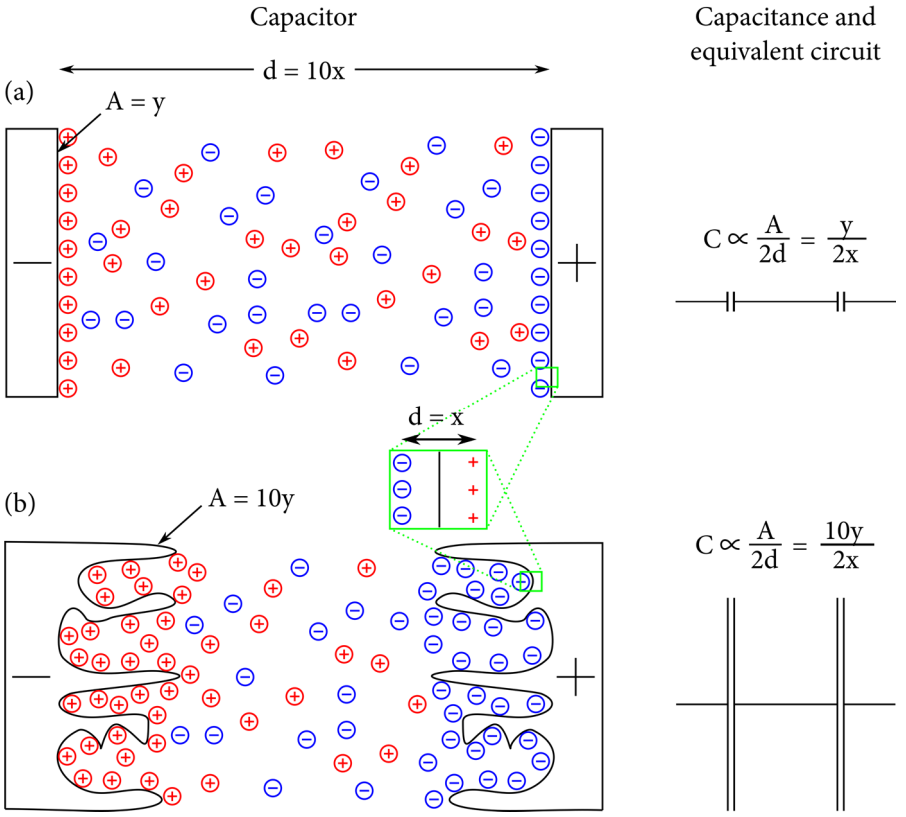


Figure 1.11. The difference in capacitance of two different biased capacitor setups if x and y remain constant. (a) The situation when the dielectric is replaced with an ICon, with mobile positive (red) and negative (blue) ions, has been drawn. EDLs are formed at the interfaces and the inset illustrates that d is now the EDL thickness, i.e. the separation between the electrode and the ions at the surface. On the right the equivalent circuit has been drawn and the capacitance that is proportional to y/2x. (b) When the electrode area is increased but the situation is otherwise similar to (a) the equivalent circuit, drawn on the right, will be proportional to 10y/2x.

thousand. Due to the fast charging mechanism of the SuCs, large amounts of current can be extracted from them quickly, making them suited for applications where sharp power peaks are required. Compared to conventional batteries, SuCs have about one tenth the energy densities, but at the same time, ten times the power density. SuCs can, however, also discharge their energy slowly making them suitable for a wide range of applications. They can serve as backup power sources for memories, microcomputers and clocks, they can serve as the main power for toys, emergency door opening and pulse power for starting of motors. They can also serve as alternating power sources where the energy is stored and used repeatedly, e.g. in solar cells during day/lamps during night or in any form of transportation where power is used during acceleration and recaptured during deceleration. The list is endless. One should, however, keep in mind that SuCs are best utilized when they are used in conjunction with other, conventional, power sources. The SuCs can e.g. handle sharp power peaks, when needed, and a leave the base power needs to the conventional battery. [68,71]

2. Experimental

The materials used to create the devices in this thesis are presented in this chapter. In Section 2.1.1 the different substrates and their preparation is described and in Section 2.1.2 the electrodes used in the transistors and supercapacitors are described. In the following Sections 2.1.3 and 2.1.4 the preparation of the semiconductors and ICons used are presented in detail. The different electrical and optical characterization methods utilized are presented in Section 2.2.

2.1. Materials and Methods

2.1.1. Substrates

The choice of substrate in this thesis has been a strong restricting factor when it comes to the possible choices of device structure, materials and fabrication techniques used, especially when it comes to the transistor. The transistor is especially sensitive to the roughness of the substrate since an uneven semiconductor layer causes trapping in the transistor channel, resulting in threshold voltage shifts, slow switching devices and increased bias stress effects. As the alternatives of environmentally friendly substrates that are also compatible with roll-to-roll (R2R) printing techniques are few, completely novel substrates have been developed at Åbo Akademi University.

2.1.1.1. PVDF

The substrate generally called the "membrane" in this thesis is the flexible, mechanically durable and chemically resistant poly(vinylidene fluoride) (PVDF). [72–74] This partially fluorinated insulator acts as the substrate for the transistors presented in **Paper I**. Several different thicknesses of the base membrane (containing different pore sizes) are available, but the membranes used in this thesis have a thickness of 200 μm and a pore size of 200 nm. The chemical structure of this material can be seen in Figure 2.1 (a). What makes this substrate novel is that it can be further functionalized to be ion-conductive and therefore also serve as ICon in the transistors. As this functionalization process can be made in selective parts, only part of the base membrane will be ion-conductive. This patterned membrane can now serve as both substrate and ICon in the DM PIMTs and EM PIMTs models presented in **Paper I**. The process is described in more detail in section 2.1.4.

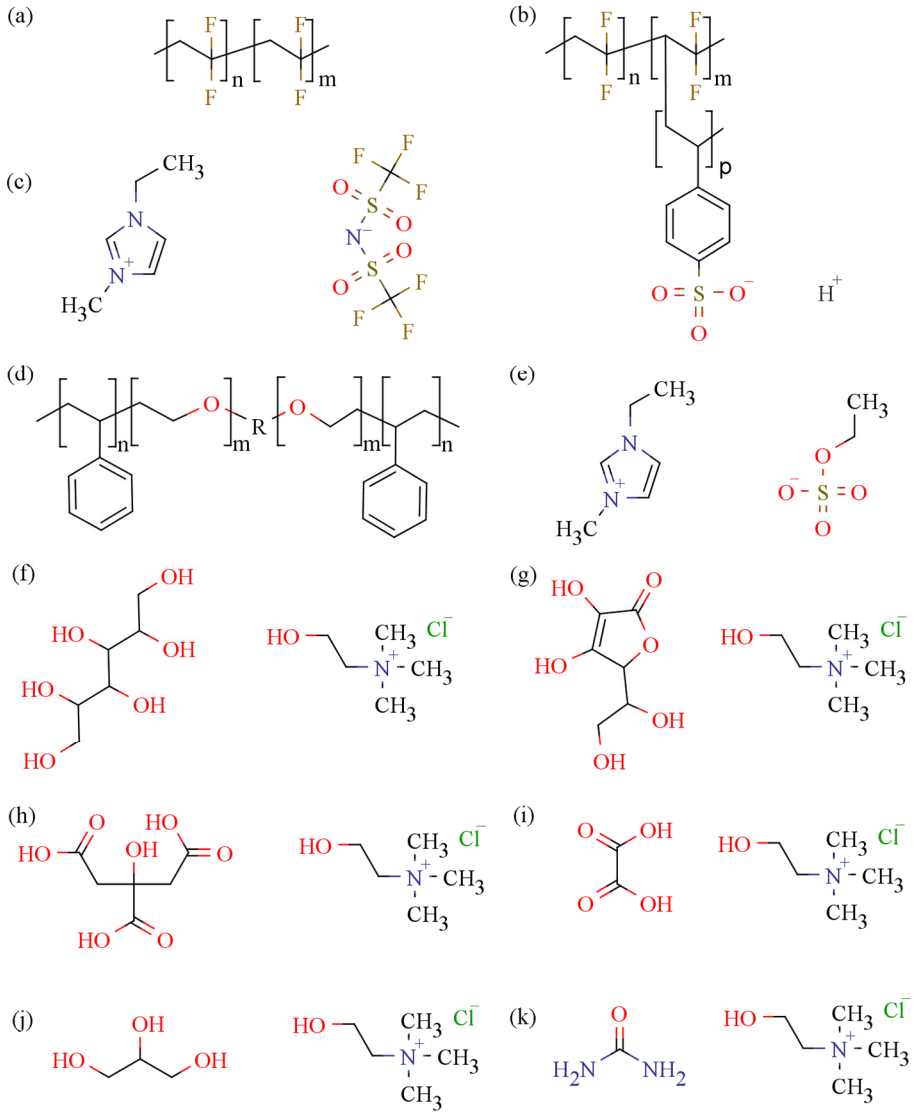


Figure 2.1. The chemical structures of the different ICons used in this thesis and some of the materials used to create them; (a) PVDF, (b) PVDF:PSSA, (c) EMIM:TFSI, (d) PS:PEO:PS, (e) EcoEng, (f) CSorb (Sorbitol + ChoCl), (g) CAsco (Ascorbic acid + ChoCl), (h) CCitr (Citric acid + ChoCl), (i) Oxaline (Oxalic acid + ChoCl), (j) Glyceline (Glycerol + ChoCl) and (k) Reline (Urea + ChoCl).

2.1.1.2. Paper

The second novel substrate used in **Papers II** and **III** is the multi-layer pigment coated paper developed and fabricated at Åbo Akademi University. [75] It has both smoothening- and barrier layers fabricated using a pilot-scale slide curtain coating technique. A pre-coated finepaper (StoraEnso Lumipress 115) was used as the base

paper and the final coated paper was calendered to achieve further smoothness. The paper contains Kaolin, mineral pigment and latex and has a surface RMS smoothness of 50-80 nm on a 10000 μm^2 area. The smoothness of the paper is close to that of Mylar A.

The paper substrate used in the "commercial" SuC structure in **Paper IV** is aluminum coated paper (Walki® Pantenna Laminate). The paper was originally developed for use as substrate for RFID-antennas and the paper has a thin coat of plastic on both sides, one of which has an aluminum coat. The aluminum serves as charge collector for the graphite/activated carbon electrodes in the SuC.

2.1.1.3. PET

Poly(ethylene terephthalate) (PET) has been used in several devices presented in this thesis. PET is a low-cost, flexible, visually clear and commercially available polyester film that is compatible with roll-to-roll fabricating processes. The PET films (Melinex 506, Pütz GmbH + Co. Folien KG) used in this thesis are 100 μm thick and have a surface root mean square surface roughness around 5 nm. Before use the films were cleaned with de-ionized water, acetone and iso-propanol in ultra-sonic baths.

2.1.1.4. Glass

Glass as a substrate has been used sparsely in the experiments in this thesis as it is not suitable for R2R-manufacturing processes nor is it otherwise suitable for low-cost, biodegradable applications. In some experiments, however, where material properties are investigated and smooth, transparent and otherwise flawless substrates are needed, glass has been chosen as the substrate of choice. Standard laboratory glass slides, cleaned with de-ionized water, acetone and iso-propanol in ultra-sonic baths, were used in those cases.

2.1.2. Electrodes

2.1.2.1. Gold

The choice of electrode material is especially critical when working with low-voltage electrolytes. The work function of the gate electrode can be changed up to 1 eV by changing the gate material, resulting in large changes in threshold-voltage. [76] As the voltage window of the transistor is comparable to the gate work function change, the transfer characteristics of the transistor will change drastically as a result. It has been shown that the shape of the transfer curve changes when the gate material (and V_T) is changed. [41,76–78] In order to maximize the subthreshold voltage swing, gold has been chosen as the gate material in the

transistors where a metal gate was used. Gold is also chemically inert, which is important when working with ICons. The source-, drain- and gate electrode material used in all transistor structures in this thesis, except in the DM PIMT and EM PIMT structures, is gold. The gold electrodes were applied using a few different fabrication methods. The source- and drain electrodes have all been applied by vacuum evaporation through suitable shadow masks. When gold was used as source and drain material in transistors in this thesis, 30 μm long and 1500 μm wide channels were fabricated. Three different methods for applying the gate electrode have been used. The first one was used in vertical transistor structures. Here, the gate electrode was applied by direct evaporation on top of the ion gel. The second one was used in lateral transistor structures. Here, the gate was applied by indirect evaporation, i.e. by evaporating gold on top of a piece of sticky tape that was subsequently attached on top of the semiconductor, on the side of the channel, prior to the ICon application. The third one was used in some experiments where the probing stations gold probe was used directly as the transistor gate electrode and no separate gate electrode was ever manufactured.

When analyzing the different ICons with impedance spectroscopy, gold was used as the electrode material in some of the experiments. Here, the same evaporation method was used as above, except that a different shadow mask was used to produce two circular electrodes of 1 cm in diameter. The electrodes were then used to sandwich the ICon being investigated to create a parallel plate capacitor.

2.1.2.2. PEDOT:PSS

Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) in water solution (1.2 wt.%) (Clevios™ P) (PEDOT:PSS) is used both as the active layer [72] and as electrode material [79,80] in the transistors presented in this thesis. See a more detailed description of PEDOT:PSS in Section 2.1.3.3.

2.1.2.3. Activated Carbon

In the supercapacitor devices (Section3.4) presented in this paper, two different types of activated carbon (AC) electrodes (the "standardized" and the "commercial" SuC) were used. The standardized electrode used was a 1×1 cm^2 reference electrode that could be used in measurements where various properties of different ICons were characterized. An important factor here is that the electrodes should be as similar as possible when, for instance, comparing the capacitance of a set of different ICons. When the electrodes for the commercial SuC were fabricated, similar pore sizes, graphite densities, electrical properties, etc. as for the standardized SuC were strived for, while having an ink that could be rotary screen printed on a pilot scale printer and result in AC electrodes that would

not delaminate during or after fabrication. The main goal here was to increase the amount of charge that can be charged to, stored on and extracted from the SuC, and to that end the electrode area was increased to 112 cm^2.

The basic aim is then, when fabricating both electrode types, to achieve as high a specific surface area (SSA) for the AC as possible. [71,81] For a typical AC, the SSA ranges between 1000 and 3000 m^2/g. [81,82] The conductivity of the electrodes is also a crucial property that needs to be optimized in order to achieve the best possible EDLs at the electrode/ICon interfaces. Therefore, a binder for the AC, suitable for this purpose, must also be chosen. Chitosan was chosen since it is biodegradable and non-toxic. [83] Although chitosan is not itself conductive, it has been shown that by mixing in enough AC the resulting blend will be electrically conductive. [84] Also, it has been shown that introducing chitosan into an AC matrix increases its carbon capture capability. [85] Another important factor to consider is the pore sizes in the electrodes. If the pores are too small, ions (or ion clusters) will have difficulty entering them, resulting in weak EDLs. If the pores are too large, the effective surface area will be small, which will have the same result. This is also a reason why different ICons, with different size and/or charge, but similar capacitances, perform differently when using AC electrodes.

Two different substrates were used for the two SuC structures; PET and paper. For the standardized SuC, PET was used in order to achieve consistent electrode properties and for the commercial SuC, paper was used in order to achieve low-cost and environmentally friendly devices. The PET substrate was laminated with a 7 μm thick aluminum layer, whereas the paper substrate had a thin plastic coat on both sides, one of which was laminated with a layer of aluminum. In both SuC structures, a layer of dense graphite (Acheson PF407A) was printed on top of the aluminum layer, in order to shield the charge collector/emitter from corrosion, as the polar ICons, used in the devices, contain water and chlorides. On top of the graphite a layer of AC (Norit DLC Super 30) is printed to serve as the active, large area, electrode. The water-based AC ink contained chitosan binder (ChitoClear fg90, Primex) in a weight ratio of 1:20.

The graphite and AC were printed using screen printers in both SuC models. The standardized version was printed on a laboratory scale, whereas the commercial one was printed using a rotary screen printer in a pilot scale printer. The same printing inks were used in both SuC structures. In the standardized version, after the graphite was printed, it was dried at 95 °C. After that a layer of AC was printed on top of the graphite layer and dried in room temperature. In the commercial SuC, the graphite was printed at 2 m/min using a screen mesh 64

threads/inch followed by 2 minutes of drying in 140 °C ovens. The AC was printed on top of that layer using the same mesh, speed and heating. The roll of electrodes was then transferred to a new machine where two extra drying steps were performed. These steps were performed at 1.5 m/min using a 5 kW IR lamp (12 seconds) and 140 °C ovens (2 minutes). These electrodes were then used, in combination with ICons (Section 2.1.3.4), to create the environmentally friendly supercapacitors presented in Section 3.4.

2.1.3. Semiconductors

2.1.3.1. P3HT

Polymeric organic semiconductors were chosen as the semiconducting material in all enhancement mode transistors presented in this thesis, as they are solution-processable at room temperature and thus compatible with R2R-compatible fabrication techniques and, most importantly, have good semiconducting properties. Solid films of organic semiconductors also have the advantage of being highly flexible, which is required for the membrane- and paper substrates used in this thesis. [86]

The charge transport occurs both along the pi-conjugated backbone of the individual polymer molecule, and hopping from molecule to molecule. [38,87] In order to make the polymer conducting, charges need to be injected into it or induced by means of chemical- or electrochemical doping. [88] All three methods can conceivably be present in one and the same transistor: by applying a gate bias, charges are injected into the SC in the channel from the source electrode; if the substrate contains OH-groups, they can penetrate and chemically dope the semiconductor; in an IMT, ions from the ICon can penetrate and dope the semiconductor during operation via electrochemistry.

The most prominent semiconductor used in the enhancement type transistors in this thesis is rr-poly(3-hexyltiophene) OS1100, acquired from Sigma-Aldrich/Plexcore, P3HT. The chemical structure of P3HT has been plotted in Figure 2.2. This semiconductor has been used in **Papers II** and **III**. It was dissolved in DCB and spray casted onto the paper substrate. It was also used to create the semiconductor/insulator blends used in the papers. The semiconductor (and insulator) was dissolved in CB before the blend was spin- or drop casted onto the paper substrate. Other, more environmentally friendly solvents that have been used to dissolve P3HT in, are p-xylene and toluene. The spray casted films were estimated to be around 300 nm thick.

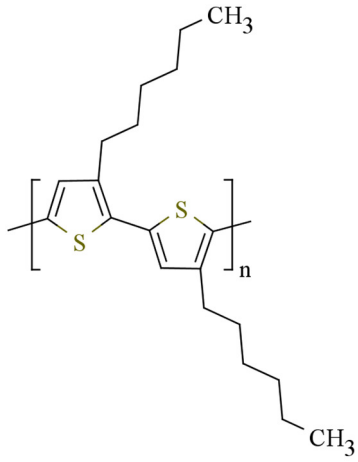


Figure 2.2. Chemical structure of P3HT.

2.1.3.2. PQT-12

Another semiconductor that has been used is poly(3,3'''-didodecyl quarter thiophene) acquired from American Dye Source Inc., PQT-12 (Figure 2.3). It has longer side chains than P3HT and is shown to have better air stability properties as well as higher carrier mobility than P3HT. [89] The electronic properties are otherwise similar to those of P3HT. [90] PQT-12 was used to create the enhancement mode transistors presented in **Paper I**. The semiconductor was dissolved in DCB and spray casted onto the membrane substrate creating roughly 200 nm thick semiconductor films.

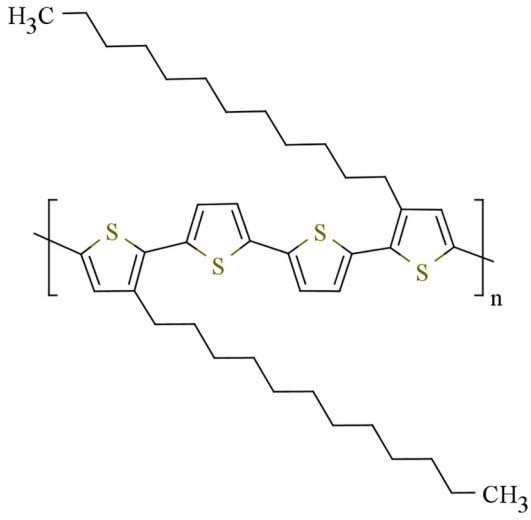


Figure 2.3. Chemical structure of PQT-12.

2.1.3.3. PEDOT:PSS

The organic redox-active (PEDOT:PSS) is conducting in its normal state [91] and must be (electro)chemically reduced in order to make it non-conductive. Due to this fact PEDOT:PSS has been used both as electrode material and the active material in the transistors presented in **Paper I**. The chemical formula of PEDOT:PSS can be seen in Figure 2.4. The positive charge carriers in $PEDOT^+$ are balanced by the counter anion in PSS^-. The concentration of polarons, responsible for the charge transport along the PEDOT polymer chains, is then dependent on the balance between neutral and reduced PSS. This situation is described by the red-ox reaction:

$$PEDOT^+PSS^- + H^+ + e^- \Leftrightarrow PEDOT^0 + H^+PSS^-$$

In its natural state (in ambient air) PEDOT:PSS has both oxidized ($PEDOT^+$) and reduced ($PEDOT^0$) parts. [91] Oxidizing it further will increase the conductivity. Over-oxidation can, however, occur at higher potentials, causing permanent loss of conduction due to permanent disruption of pi-conjugation. [92–94] Reversible reduction, on the other hand, is accomplished by the addition of protons and electrons, i.e. by reducing the amount of polarons available for charge conduction. To increase the conductivity, a small amount of ethylene glycol (typically 5%) has been added to the PEDOT:PSS/water solution. The reason for this has been explained as a better ordering of the conducting PEDOT:PSS chains, and expulsion of the non-conducting PSS groups, during the solvent evaporation process. [80,95,96]

All PEDOT:PSS layers presented in this thesis are applied by drop casting. The layout of the gate and channel (including source and drain electrodes) of the DM PIMT can be seen in Figure 1.6. During operation the protons move between the gate PEDOT:PSS and channel PEDOT:PSS, simultaneously reducing one and oxidizing the other, depending on the external electron flow supplied by an external power source. The DM PIMT has the gate electrode ionically connected to the channel, via the patterned membrane's poly-electrolyte, so that the gate PEDOT:PSS acts as a conductor and the channel PEDOT:PSS as active material. The gate area is about ten times larger [97] than the channel area (defined as the PEDOT:PSS in contact with the ICon). This is done so that the channel can effectively be reduced without over-oxidizing the gate PEDOT:PSS. Also, the thinner the channel PEDOT:PSS layer is, the easier it is to reduce it and re-oxidize it during operation.

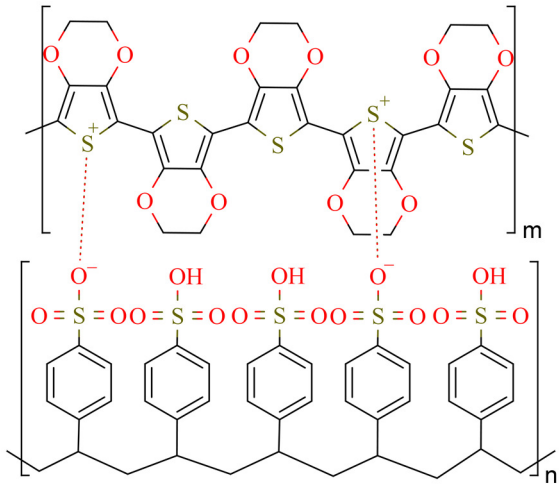


Figure 2.4. Chemical structure of PEDOT:PSS.

2.1.3.4. Blends

In **Paper II** different concentrations of poly(3-hexylthiophene):poly(L-lactic acid) (P3HT:PLLA) blends were used to create vertically phase-separated semiconductor/insulator (SC/INS) layers [98] in the transistor, in order to speed up the device switching speeds. The basis for this idea was that by replacing the pure semiconductor layer with a SC/INS layer the thickness of the SC would be reduced. The advantage of this is that the electrochemical process that occurs during transistor operation will be faster when the SC layer is thinner. The electrochemical doping of the SC will be faster, if the ions penetrating it have a shorter distance to travel, which is the case when the SC layer is thinner. As a result of this the switching of the transistor will be faster. As we are aiming towards environmentally friendly devices, the polymer insulator PLLA (124000 g/mol, HM1011, T&L Finland Oy) was chosen as it is biodegradable, non-toxic and cheap. [99] The chemical structure of PLLA can be seen in Figure 2.5.

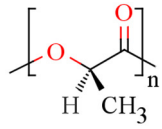


Figure 2.5. Chemical structure of PLLA. Substituting the positions of the hydrogen, going into the page, and carbon, coming out of the page, would create the other chiral form of PLA, namely PDLA.

Other physical demands were also required of the insulator; it had to be solvable in the same solvent as P3HT, it had to have suitable surface energies compared to that of P3HT and the paper substrate, and finally, its solubility (in the chosen solvent) had to be lower than that of P3HT. All of the above mentioned requirements were fulfilled by PLLA and the solvent chosen was chlorobenzene (CHROMASOLV®, for HPLC, 99.9%, Sigma-Aldrich) (CB). PLLA is a mixture of poly(lactid acid) in both L- and D-chiral forms. The mixture used is 95 mol% L-form and 5 mol% D-form. Other concentrations were also tested but resulted in either badly performing devices or materials that would not dissolve in CB. A more detailed analysis of the blend is made in Section 2.1.3.4 and **Paper II**.

The insulator and semiconductor were both dissolved separately in CB with 2 wt% concentration. They were then mixed together and heated at 70 °C for 10 minutes before application. Several different P3HT:PLLA concentrations were made in order to perform all the different experiments presented in **Paper II**. They ranged from 0.2:99.8, 0.5:0.99.5, 0.8:99.2, 2:98, 5:95, 10:90, 20:80, 30:70, 50:50 to 70:30 for the different AFM thickness- and phase-, XPS-, water contact angle-, rise time-, transistor-, inverter- and ring-oscillator measurements. The blends were spin casted at 450 RPM for 18 s + 750 RPM for 60 s and subsequently dried at room temperature for two hours. In **Paper III** a blend concentration of 20:80 was used and applied by drop casting. This was done to demonstrate that the blend can be applied using R2R-compatible fabrication methods. The drop casting was done so that the sample was kept at a 45° compared to the horizon and the blend was dropped from a height of 5 cm above the sample. The films were subsequently dried at room temperature for two hours. All blends were applied in an inert atmosphere.

2.1.4. Ion-Conductors

The ICons that have been used in this thesis are many and vary among other things in ionic-, chemical-, electrochemical-, mechanical- and environmental properties. They are, apart from electrodes, the only common denominator in all the devices: transistors, inverters, oscillators, gates and supercapacitors alike, presented in this thesis. The main advantage of using ICons in transistors instead of ordinary OFET dielectrics is the high capacitances, and thereby low-voltage operation, that are achievable. [14,59,100–102] And since they are potential driven they are also less sensitive to substrate roughness, as the thickness does not affect the total capacitance, [53] a property well suited for working with paper.

In **Paper I** the ICon used is poly(vinylidene fluoride) poly(styrene) sulfonic acid (PVDF:PSSA). [72–74] This ICon is perhaps the one most divergent from the other ones used in the thesis in all categories. To begin with, it starts off

as PVDF, a 200 μm thick, flexible, self-supporting and non-conductive, membrane that is further functionalized, through an EB process previously reported by others [45,72–74] to be ion-conducting in selectable places. This process includes three major steps: an electron beam irradiation step, a grafting step and a sulfonation step. Thus, the resulting membrane contains both insulating- (PVDF) and ion-conducting parts (PVDF:PSSA), distributed on the membrane according to the shape of the shadow mask used in the first, electron beam irradiation, step. The patterned membrane is a continuous film with the PVDF:PSSA parts perturbing slightly out of the membrane plane due to an increase mass during the functionalization process. The brittleness of the membrane slightly increases due to this process, as is shown in **Paper I**, but the membrane still remains mechanically robust. The chemical structures of PVDF and PVDF:PSSA have been drawn in Figure 2.1 (a) and (b), respectively. The sulfonate anion, SO_3^-, is covalently bound to the polymer backbone and immobile, while the counter-ion, H^+, is free to hop between SO_3^- anions. The ICon is, in fact, a poly-electrolyte and behaves according to the description given in Section 1.2.2.

The enhancement- and depletion mode transistors presented in **Paper I** use the patterned membrane both as substrate and ICon. The patterning can thereby be tailor-made to fit many different logic circuit designs. As the ICon parts of the membrane go all the way through the membrane plane, they can be used to minimize the need of artificial vias that would otherwise be needed, especially in more complicated logic circuits.

In **Paper II** a liquid or gelatinized IL was chosen as the ICon. This 1-Ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide (EMIM:TFSI) was chosen as it had shown to have the highest capacitances and to be quickly polarizable in an external electric field. [61,90,103–105] It is also referred to as the state-of-the-art ICon in **Papers III** and **IV**. The chemical formula of the IL can be seen in Figure 2.1 (c). The EMIM:TFSI was purchased from Sigma-Aldrich and gelatinized with the triblock copolymer poly(styrene-b-ethylene oxide-b-styrene) (Sigma-Aldrich) (PS:PEO:PS) (7 wt%). PS:PEO:PS (Figure 2.1 (d)) was first dissolved in ethyl acetate followed by the addition of the IL. The ion gel (IG) was finalized by evaporating the ethyl acetate on a hotplate (70 °C) for 24 h. This IG had the viscosity close to that of honey. At room temperature it remained in liquid form when used as ICon (in a drop form) in the transistors presented in **Paper II**. When EMIM:TFSI was used as the reference ICon in the SuCs presented in **Paper IV**, there was no triblockpolymer present as the IL was used as purchased. In the SuCs, the ICon was drop casted directly onto the AC electrodes (1 cm^2 and 56 cm^2), after which the air bubbles in the AC were forced out using vacuum or by waiting

for the bubbles to clear from the ICon, returning it to a clear liquid. The SuCs, including the application of the ICon, were assembled in air.

This immidazolium IL, however, contains harmful fluorinated groups. We therefore turned our attention towards a group of similar materials, namely deep eutectic mixtures (DEMs). [106–108] DEMs are mixtures of quaternary ammonium salts and metal salts or other complexing agents that are mixed at a molar ratio that gives the lowest melting point (eutectic point). This melting point should also be under 100 °C. They are separate from ILs that only contain discrete anions. DEMs can be made to be more environmentally benign than the immidazolium ILs, if the materials are chosen wisely. The DEMs presented in **Papers III** and **IV** are based on (2-hydroxyethyl) trimethylammonium chloride (ChoCl). ChoCl can be found on the list of allowed food additives [109–111] and is present in the biochemical cycle of live organisms (3a890). ChoCl is a solid at room temperature (melting point: 302 °C), but when mixed with e.g. Sorbitol (melting point: 98 °C) results in a DEM, being a liquid at room temperature. Sorbitol is just one of several different environmentally friendly organic compounds that were used to create the DEMs with. Other complexing agents, including amides, acids and sugar alcohols, were also used. They were: Urea (E927b), Oxalic acid (no E number), Citric acid (E330), Ascorbic acid (E300), Glycerol (E422) and Sorbitol (E420). The DEMs Reline (Urea + ChoCl), Oxaline (Oxalic acid + ChoCl) and Glyceline (Glycerol + ChoCl) were all purchased ready made from Scionix Ltd. and were used as bought. Citric acid + ChoCl (CCitr), Ascorbic acid + ChoCl (CAsco) and Sorbitol + ChoCl (CSorb) were bought separately from Sigma-Aldrich and mixed together in 1:1 molar concentration. A commercially available state-of-the-art "green" ICon (1-ethyl-3-methylimidazolium ethylsulfate, 99 %, Solvent Innovation GmbH (EcoEng)) was also used to create reference devices with, in order to compare the performance of the DEMs to. The chemical structures of EcoEng and the DEMs have been plotted in Figure 2.1 (e) – (k). The IL EcoEng and the DEMs were used and handled in the same way as EMIM:TFSI was in the transistor- and the SuC structures, apart from the fact that some of these (CCitr and CAsco) had to be heated to 60 °C in order to improve the handling (decreased viscosity).

The ILs and DEMs were handled in an inert atmosphere when the transistors and transistor-based devices were manufactured and measured and in an ambient atmosphere when SuC devices were manufactured and measured. The ILs and DEMs were also further mixed with a commercially available water-based binder (20:80 wt%) to create solid ICon layers in the completely solid transistors presented in **Paper III**. After spin casting the ICon, the layer contains roughly 50 % IL or DEM and 50 % binder. The binder is simply there to provide a matrix for

the liquid IL or DEM to reside in. The films were spin casted at 3000 RPM in an inert atmosphere, except in the "integrated circuit" SR-latch presented in **Paper III**, where a drop of solution was placed beside every channel and a piece of paper was used to create a flat ICon layer over the channel area.

2.2. Measurements

2.2.1. Electrical Characterization

2.2.1.1. Current-Voltage Measurements

A large number of different types of current-voltage measurements have been carried out during the projects that eventually lead to the compilation of this thesis. The different measurements have been done using several instruments in different combinations. A general theme has been that the instruments have been controlled with a personal computer and suitable software has usually had to be written to accommodate for all the different types of measurements that have been done. The most used programming software platform has been LabVIEW. The most used instrument is the Agilent 4142B Modular Source/Monitor, with three 41421B S/M units and one 41420A S/M unit, as it is used in all typical transistor characterization measurements, i.e. output-, transfer-, rise time- and bias stress measurements. A probing station is usually used to connect the transistor device to the Agilent measuring instrument. The probing station consists of three gold spring contact probes that are equipped with magnetically mounted vertical linear stages. The reason for using gold probes is that this material is chemically stable and has a suitable work function e.g. for injecting charge carriers into the semiconductors used in this thesis. Two separate models of Keithleys were also used in a number of different measurements. The models used were the 2400 SourceMeter and the 2612 System SourceMeter. These were used, both in the logic circuit measurements (NOR-gates and SR-latches) in **Paper III** in addition to the Agilent 4142B, where more than four channels were needed, as well as in the constant current cyclic charge discharge measurements of SuCs in **Paper IV**.

Two separate pairs of measurement setups were used to measure the inverters and ring-oscillators presented in **Papers I**, **II** and **III**. In most cases, one pair was used for fast-switching devices and another pair for slow-switching devices. The outputs of the inverters and ring-oscillators, in both cases, were connected to a unit gain amplifier, built using an AD8642 operational amplifier, in order to avoid putting stress on the device being measured. For the slow measurements, the Agilent 4142B was fast enough to do the measurements with, whereas for the faster measurements (>1 Hz), a different setup was needed, in

order to be able to see the fast oscillation of the devices. For instance, the inverter measurements presented in **Paper III,** were done using an Agilent E3631 Triple Output DC Power Supply, a Stanford Research Systems Model DS345 Synthesized Function Generator and a Tektronix TDS 2002 Two Channel Digital Storage Oscilloscope. These measurement setups were most commonly used when characterizing the transistors, inverters and ring-oscillators in **Papers I**, **II** and **III**. In order to more easily be able to characterize the more complicated circuits (NOR-gates and SR-latches) in **Paper III**, integrated circuitry was created. This entailed pre-connecting up to four separate transistors during the fabrication process (by means of using suitable shadow masks when evaporating the interconnections and transistor electrodes) resulting in a lesser number of connections needed when eventually characterizing the finished device. The terminals of the logic gates were also positioned on the substrate in such a way, that the device could easily be fitted into pre-existing clamps (like a plug into a socket) that were connected directly to the measuring instruments.

2.2.1.2. Impedance Spectroscopy

Impedance spectroscopy (IS) [112] is a powerful tool for investigating otherwise inaccessible electromagnetic and electrochemical properties of a wide range of electrical circuits and materials, including electronic devices, composite materials, paints, rust, etc. The property that is being measured with IS is the opposition the cell, i.e. the device being measured, presents on the current when a voltage is applied over it. This is called the impedance, Z. An alternating voltage is applied and the current response is measured by the instrument. The phase-shift, θ, between the sinusoidal input voltage and -output current and the ratio between their amplitudes, i.e. the magnitude, |Z|, is reported by the instrument. It is often useful to write these in complex form:

$$Z = |Z|e^{i\theta} \text{ (polar)} \tag{2.10}$$

$$Z = R + iX \text{ (Cartesian)} \tag{2.11}$$

where R is the resistance (real part of the impedance) and X is the reactance (imaginary part of the impedance). The relation between the two forms of the complex impedance can be visualized graphically as shown in Figure 2.6. An ideal resistor will only possess real impedance while an ideal capacitor will only possess imaginary impedance.

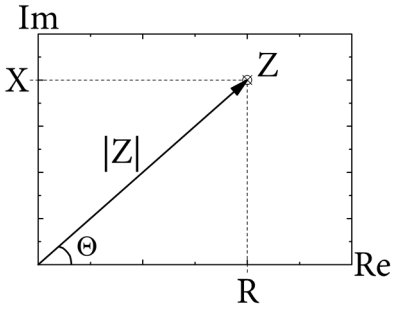


Figure 2.6. Graphical relation between the Cartesian- and polar representations of the complex impedance.

IS is sensitive to all forms of charge present in the cell being measured, e.g. electrons, dipoles and ions. All charged species will react to the changing electric field over the cell, and thus, all forms of charge relaxation and electrochemical processes will be detected by the measuring system. This is the most advantageous feature of IS, but at the same time also the most problematic. The reason is that it can be very difficult to determine the origin of many of the observed signals. For this reason a large part of the IS analyzing procedure includes fitting the measured data to appropriate equivalent circuits. Knowledge of the basic composition of the system being measured is, therefore, a crucial part of the measurement procedure. Further, IS is measured over a wide range of frequencies. This is a good way to determine whether the signals being measured originate from dipole changes or electronic- or ionic motion, for instance, as these respond very differently to electrical signals of different frequencies. Typical ways to present the measured data is in the form of Nyqvist plots, Bode plots or just the fitted capacitance, conductivity or resistance as a function of frequency. When analyzing SuCs, for instance, the capacitance and internal resistance are most important, as these determine how much charge can be stored in these devices and how fast they can be charged or discharged. The internal resistance can be read as the real part of the impedance directly from the Nyqvist plot while the capacitance is a function of the imaginary impedance, frequency and surface area of the capacitor.

In a SuC with an ICon containing positive and negative ions, the capacitance is higher at low frequencies and diminishes towards higher frequencies. The reason for this is that the ions are slow to move and cannot respond to a fast-oscillating signal, whereas at low frequencies the ions have time to move and a high capacitance can be measured. The internal resistance operates in an opposite fashion where the SuC behaves as a pure resistor at high frequencies. The instrument used to perform the IS measurements in this thesis is a Gamry 600 Impedance Spectrometer. All measurements were performed in tripolar

potentiostatic mode with 0 V bias and an rms signal amplitude of 20 mV. The frequency range was set between 1 Hz and 1 MHz.

2.2.2. X-Ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) [113] is a method where a sample being analyzed is irradiated with an X-ray and the amount and kinetic energy of the escaping electrons are measured. XPS can be used to determine the empirical formula, chemical state and electronic state of a material. The electron binding energy is simply the kinetic energy of the escaped electron subtracted from the energy of the x-ray. The output of the instrument is a spectrum of binding energies of all electrons detected, with each peak corresponding to a specific electron orbital of a specific atom, e.g. O 1s, Si 2s and N 2p. The composition of the material can then be deducted based on the measured spectrum. The instrument has a detection limit of about one part per thousand. It is sensitive to the first 10 nm of a sample and, utilizing e.g. sputtering in between consecutive measurements on a specific spot, a depth profile can be measured using the instrument. The instrument was used e.g. to measure a depth profile of a P3HT:PLLA film, spin casted on PET. The instrument used was a Physical Electronics Quantum 2000 scanning spectrometer using an Al Kα x-ray (1486.6 eV) source.

2.2.3. Contact Angle- and Optical Measurements

A few different optical measuring techniques have been utilized to better understand the bulk and surface of the pure P3HT semiconductor and the semiconductor/insulator blend. The most frequently used instrument was one of many optical microscopes available, mainly for examining casted and evaporated films, but also to determine the phase-separation of the blend and analyzing the crystallinity of different concentration P3HT:PLLA blends. Water contact angle measurements were used to estimate the surface energies involved when casting the blend onto different substrates and also to estimate the semiconductor coverage on the surface of semiconductor/insulator blends. The method involves applying a water droplet on a surface being investigated and measuring the shape of the droplet. The hydrophobicity of the substrate, dependent on the surface energy, will change the shape of the droplet. The instrument used was a KSV Instruments contact angle meter. Other less used optical measurement instruments in this thesis are ultraviolet-visible spectroscopy and confocal optical white-light microscopy. These were used e.g. to analyze the P3HT:PLLA blend and the surface roughness of the SuC AC electrodes.

2.2.4. Atomic Force Microscopy

Atomic Force Microscopy (AFM) is an instrument that uses a wide variety of forces to determine e.g. the topography of a given substrate. The instrument applies a tip to the sample and simultaneously measures the resulting motion of the tip. The forces associated with the interaction between the tip and the sample includes mechanical contact, van der Waals forces, electrostatic forces, Casimir forces, magnetic forces, etc. AFM has a resolution down to about 1 nm, depending on the instrument and atmospheric conditions. AFM has been used to measure the thickness and surface roughness of substrates and semiconducting-, insulating- and conducting films. It has also been used to determine the surface distribution of semiconductor and insulator films in different concentration P3HT:PLLA blends. The phase images were here used to do this determination, as the topography images did not reveal any visible features that could be used to distinguish between the semiconductor and the insulator. The phase images give information on the softness of the surface [114] being scanned and it turned out that they are different enough for P3HT and PLLA that a distinction between them could be made. The instrument used is a Veeco diCaliber AFM.

3. Results and Discussion

This chapter is devoted to presenting the main results of this thesis. The chapters are named after the individual articles and covers electronics built on a patterned ion-conducting membrane, the move towards a paper substrate and the development of the semiconductor/insulator blend, making environmentally friendly logic on paper and finally building environmentally friendly paper-based energy storage units.

3.1. Patterned Membrane as Substrate and Electrolyte in Depletion- and Enhancement Mode Ion-Modulated Transistors

This section is based on the main results presented in **Paper I**. The EM PIMT and DM PIMT presented in this chapter are both built on the same patterned PVDF:PSSA membrane. Both transistors can be fabricated in any combination on the same substrate, simultaneously, and therefore separate transistors, inverters and ring-oscillators have been fabricated using both transistor types in order to demonstrate the viability of this patterned membrane platform.

Typical output curves of EM PIMTs and DM PIMTs can be seen in Figure 3.1. The curves show moderate transistor properties, the most critical being the poor on/off-ratios and slow switching speeds, even when compared to traditional OFET properties. Nevertheless, these devices are manufactured on a cheap flexible membrane using R2R-compatible fabrication techniques. Applications in where speed is not the most important factor and e.g. cost and recyclability are more important, these devices can potentially be used. Also, the same patterned membrane platform can be used to build other devices, e.g. energy storage units or electrochemical displays. [45] A wide range of devices can thus be fabricated using the same membrane and the same materials, reducing the amount of fabrication steps and thereby the total cost of the device in question. To demonstrate that basic electronic devices in fact can be built using these types of devices more complicated circuits were fabricated, i.e. inverters and ring-oscillators. The structure of an inverter in depletion mode built using both an EM PIMT and a DM PIMT is illustrated as inset in Figure 3.2 (a). In theory, larger amplification can be achieved with the inverter operating in depletion mode than in enhancement mode. The most important factor to observe here is that the output of the inverter is larger in amplitude than the input. This is required when

building a circuit with more than one inverter. Another important factor is the speed at which the device inverts. Also, the power consumption of any electrical device is important and, thus, the drive voltage at which the inverter amplifies is critical.

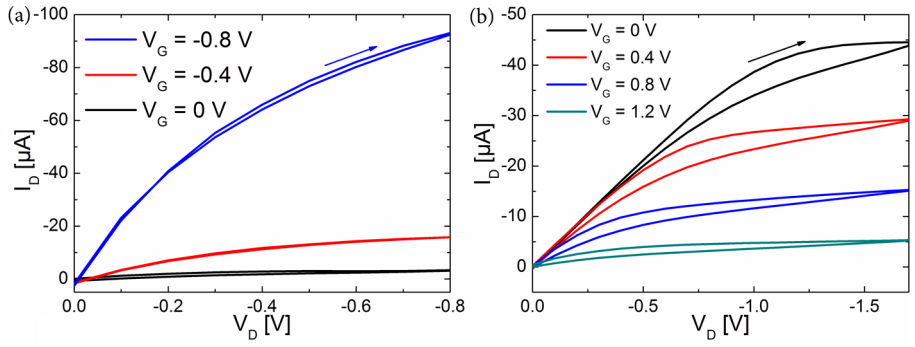


Figure 3.1. Typical output curves of the (a) EM PIMT and the (b) DM PIMT. The main difference between the two is that the source-drain current ***increases*** *in the EM device when increased negative gate biases are applied, while in the DM device the source-drain* ***decreases*** *when increased positive gate biases are applied. The DM device is also slower to turn off and on, due to the fact that the channel is electrochemically reduced and oxidized in order to complete those processes, whereas in the EM device no electrochemistry occurs in the semiconductor during operation.*

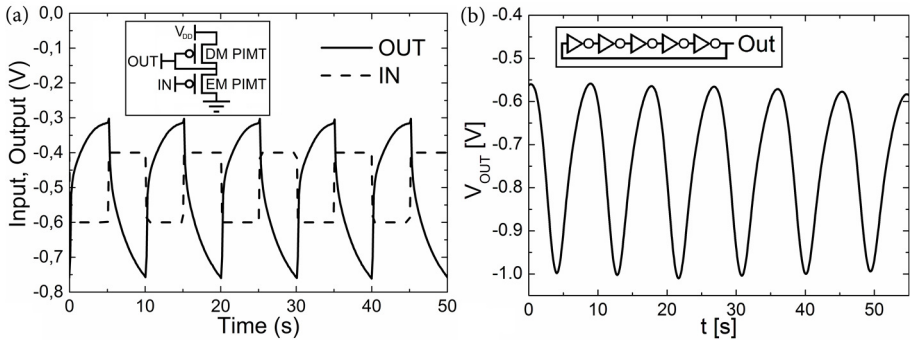


Figure 3.2 (a) The input and output of a depletion mode inverter made up of an EM PIMT and a DM PIMT operating with a -2 V drive potential. The device setup can be seen as inset in (a). Using five of these inverters a five-stage ring-oscillator was constructed and its output can be seen in (b). The oscillator setup has been drawn as an inset in the figure.

The inverters built using these devices typically operate below -2 to -2.5 V. Finally, a five-stage ring-oscillator built using ten transistors (both EM- and DM PIMTs) is demonstrated. Generally, a ring-oscillator setup can be used to demonstrate that a particular inverter can be used as building blocks in electronic devices. Also, the

switching speed of the inverters used can be estimated. The output of the oscillator can be seen in Figure 3.2 (b), and the device structure used can be seen as inset in the same figure. The oscillation frequency of this device was roughly 100 mHz and the propagation delay time per inverter-stage was calculated to be about 1 second.

Even though these devices are operated in air, their electrical properties are greatly affected by the atmosphere humidity. These effects include changes in transistor switching speeds, on- and off-current levels, degree of saturation, etc. These, in turn, affect the more complicated devices built using these transistors, i.e. inverters and ring-oscillators, in a way that is observed as a change in signal output amplitude and level and in oscillation frequency. There are a few reasons for these observed variations: firstly, the ion mobility is changed when more water molecules are present in the poly-electrolyte, [74] secondly, the PEDOT:PSS conductivity changes as a function of humidity in the atmosphere, [115] thirdly, an increased trap density at the semiconductor interfaces is expected in a moist atmosphere. [116] It has also been observed that these devices will not operate correctly in a completely dry atmosphere. [117] The poly-electrolyte e.g. will have very low ion-conductivity in those conditions. The solution can be to operate these devices in a fairly controlled atmosphere, incorporate different encapsulation techniques or use the same devices as humidity sensors and compensate for the humidity effects in some clever way.

The main result demonstrated here is that the membrane can be used as a platform for different electronic devices, while simultaneously operating as an active component in the transistors. As some of the transistors' electrodes can be placed on either side of the membrane, building additional vias can completely be avoided by clever circuit design. Logic circuits using up to ten transistors have been demonstrated using the patterned membrane as the platform.

3.2. Ion-Modulated Transistors on Paper using Phase-separated Semiconductor/Insulator Blends

Using paper as a substrate brings a whole new set of challenges, but also opportunities. The paper used in this thesis is a multi-layered paper developed at Åbo Akademi University. The main features that the paper has that is important for building electronics on it is that it has a barrier layer that keeps most of the water out and limits the amount of semiconductor-absorption and that it has a smoothening layer that reduces the degree of roughness of the semiconductor layer. Nevertheless, this novel paper substrate was not a solution for all the

problems associated with solution-processable deposition techniques, only a good base where to start solving the problems from.

The biggest problem when attempting to solution deposition a semiconductor onto the paper substrate is that there will always be some degree of absorption into the paper substrate. This results in a semiconductor layer that is thick and uneven (at least as uneven as the paper surface). This can be very problematic when working with low-voltage organic transistors. The solution is therefore to use an ICon layer instead of the traditional dielectric layer. An ICon is less sensitive to substrate roughness as it is potential driven instead of field-effect driven. This means that the ICon layer can be much thicker than a dielectric layer would have to be, in order to reach the same degree of capacitive coupling between the gate and the channel. The results presented here are mainly based on **Paper II**.

The problem with using an ICon turned out to be that the devices were very slow to switch between off-state and on-state. The current levels, however, turned out to be enormous in on-state and on/off-ratios of 10^6, were easily achieved. We demonstrate a five-stage ring-oscillator fabricated on paper that oscillates ten times every day. This translates to a propagation delay time of 870 seconds. The structure of the individual transistors used in the ring-oscillator and the actual output of the device can be seen in Figure 3.3. The ring-oscillator is one of the first solution processed on a paper substrate not coated with plastic.

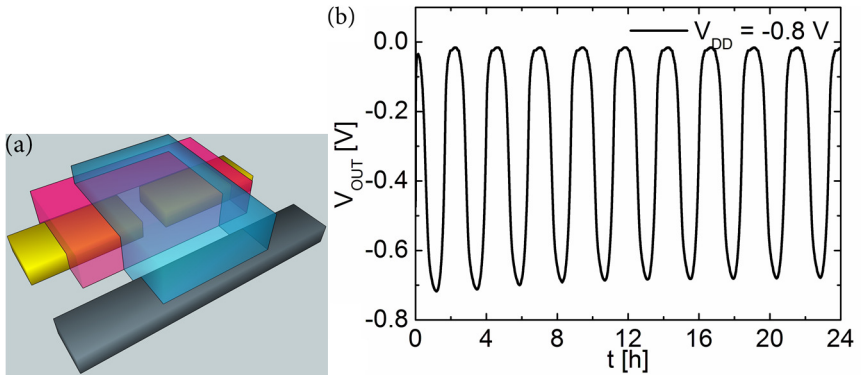


Figure 3.3. (a) Device structure of the lateral IMT. The pink semiconductor spray casted on top of the gold source and drain electrodes is about 200 nm thick. The blue ICon covers the channel area and the silver gate. (b) The output of the ring-oscillator constructed of inverters made of transistors shown in (a).

The transistors used for creating this slow switching device were lateral ion-modulated transistors (IMTs). The high currents and slow switching speeds indicate that the very thick semiconductor is being penetrated by ions from the

ICon during operation. The ions electrochemically dope the semiconductor which results in a large source-drain current. As the bulk of the semiconductor is being doped and de-doped during operation, it takes time for the ions to penetrate the entire bulk of the thick semiconductor. This results in devices having large on-currents but also having slow switching speeds.

A direct solution to the problem of ions penetrating the semiconductor could be to evaporate a thin ion-blocking layer on top of the semiconductor. Whatever the result of this solution, it would entail one extra non-R2R-compatible fabrication step. A second work-around would be to allow for the electrochemistry but making the semiconductor layer thin. This way the electrochemical doping of the semiconductor during operation would be fast, as the semiconductor layer would be very thin. On a paper substrate, however, fabricating a thin semiconducting layer is close to impossible. There will always be some absorption into the paper making it impossible to achieve very thin layers.

Here we have utilized the method of spontaneous phase separation [98] of a semiconductor/insulator blend during the deposition step. The semiconductor and insulator are both dissolved in CB before the casting process. The semiconductor and insulator used are presented in Section 2.1.3.4. The blend is then either spin casted or drop casted onto the paper substrate and due to favorable solubilities and surface energies of the paper substrate, semiconductor and insulator, the insulator will precipitate first and form a layer on the paper leaving a thin layer of semiconductor on top. A drawing of a pure P3HT film casted on paper has been compared to the a blend casted on the same substrate in Figure 3.4.

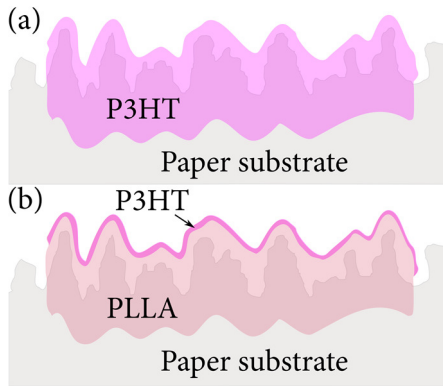


Figure 3.4. (a) A drawing of pure P3HT solution-casted onto a paper substrate. (b) A drawing of a small concentration of P3HT in PLLA solution-casted on the same substrate. The P3HT forms a layer on top of the PLLA.

We demonstrate the effect of utilizing this spontaneous phase separation to achieve a thin semiconductor layer in transistors fabricated on paper by measuring the raise time of said transistors and plotting them as a function of semiconductor concentration (Figure 3.5). The concentration of semiconductor corresponds to the thickness of the semiconductor layer. It is clear that the rise time of the transistors increase with increasing semiconductor layer thickness. This means that a thicker semiconductor layer takes more time to electrochemically dope than a thinner one. What is also noticeable is that the effect is significant for already small increases in the layer thickness (e.g. at 10 %: $\tau = 10$ s while at 20 %: $\tau = 100$ s).

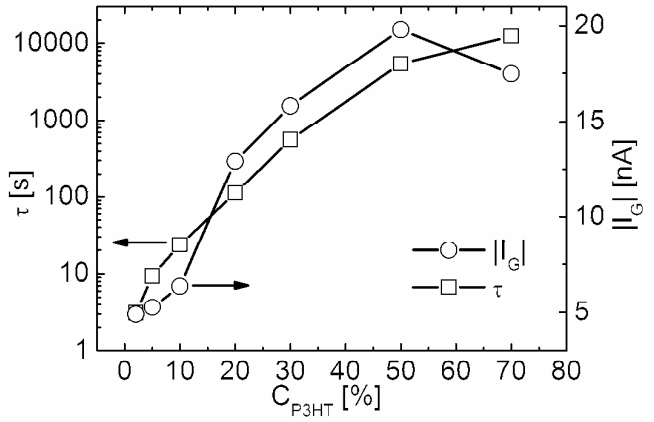


Figure 3.5. The measured rise time, τ, of transistors constructed of different concentration semiconductor/insulator blends. τ is plotted as a function of semiconductor concentration, C_{P3HT}. The gate-leakage in on-state, I_G, has also been plotted. The observed increase can be a result of the decreased insulating layer between the electrolyte and the source- and drain electrodes and/or increased displacement current caused by increasing amount of ions moving into the semiconductor.

It turns out that this method of phase separation is the first really simple and R2R-compatible way of fabricating fast switching transistors on a paper substrate. This method is also robust in the sense that the yield of fabricating transistors with similar electronic properties, even by hand is really high. Moving towards mechanized fabrication methods would further improve the yield. This technique really opens up the possibility of building more complex electronics on the flexible paper substrate. As a demonstration of this an operating ring-oscillator has been demonstrated using three inverters built with transistors containing the phase-separated semiconductor/insulator blend. The output of this ring-oscillator can be seen in Figure 3.6. The propagation delay time of this device was calculated

to be around 35 ms. Compared to the earlier pure-semiconductor device, this a more than four orders of magnitude increase in speed.

A large part of the semiconductor is here replaced with the bio-degradeable polymer insulator. Concentrations down to 0.5 wt% of P3HT:PLLA blends have been used to create functioning transistors with. Reducing the amount of potentially hazardous and expensive semiconductor used in each device and the fact that the fabrication process is R2R-compatible will result in cheaper fabriction costs and increase the the bio-degradability.

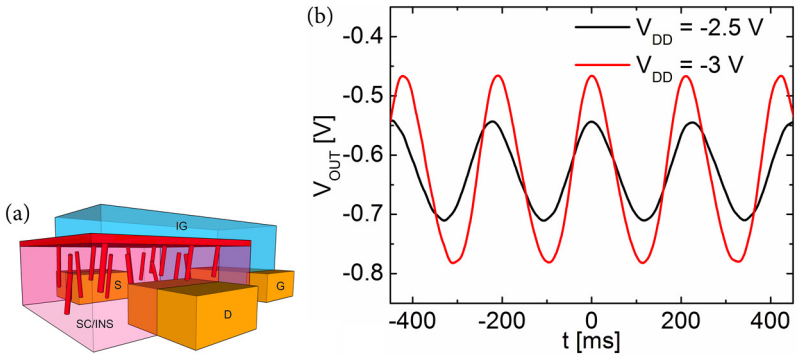


Figure 3.6. (a) The device structure of a blend device. The phase-separation of the semiconductor and insulator has been emphasized with red semiconductor and pink insulator. Laterally phase-separated semiconductor strands ensure conduction paths for charge injection into the vertically phase-separated semiconductor layer on top, from the source and drain electrodes. The gold source, drain and gate electrodes are marked with S, D and G, respectively. The ICon is marked with IG. (b) The output of a three-stage ring-oscillator constructed of blend transistors. The oscillation amplitude and frequency can be controlled by the drive voltage, V_{DD}.

3.3. Environmentally Friendly Transistors and Circuits on Paper

So far, the IL EMIM:TFSI, in gel- or liquid form, has been used as the ICon layer in the transistors. Although this ICon has favorable electronic and ionic properties, it is hazardous for the environment. A substitute with similar electronic properties, but more environmentally friendly chemical properties than this IL is therefore required. In **Paper III** this issue is addressed and the main results are presented in this chapter. The DEMs presented in Section 2.1.4 are here used as the ICon layer in our paper transistors. The semiconductor/insulator blend used has a concentration of 20 % semiconductor to insure high-enough operating currents while simultaneously keeping the switching speeds as low as possible. The different

ICons are then investigated in different transistor setups to clarify the effect of the substrate used, the semiconductor layer used and the hardness-state of the ICons themselves. Using the 100 % semiconductor layer and PET as substrate, it was clear that the EcoEng IL, used as a the commercially available, state-of-the-art "green", reference ICon, performed the worst compared to all of the investigated ICons. The ICons were then used to fabricate devices on the paper substrate and also using the semiconductor/insulator blend. Using the blend here is necessary since devices fabricated on paper using 100 % semiconductor are impossibly slow, as described in Section 3.2. The main conclusion that could be made here was that the CSorb (DEM) device stood out as the best transistor to use when creating environmentally friendly electronics on paper. The final step that had to be made, for practical reasons, was creating a solid ICon. We then use a commercially available, water-based binder to solidify the ICons with. The devices are now completely solid with the gate evaporated on top. The final device structure can be seen in Figure 3.7.

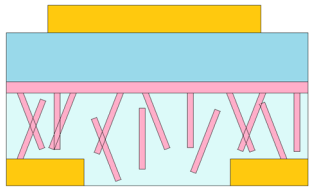


Figure 3.7. The solid vertical transistor structure with gold source- and drain electrodes at the bottom, pink and light blue semiconductor/insulator blend, blue ICon and gold gate on top.

The same conclusion held true after the solidification of the ICon, namely, the CSorb device clearly outperformed all the other devices, including the commercial reference IL. The output- and transfer curves of the CSorb transistor can be seen in Figure 3.8 (a) and (b). The electronic properties of this CSorb transistor are now good enough so that actual electronic logic circuits can be fabricated on the paper substrate. The on/off-ratio of 7200, sub-threshold voltage swing of 280 mV/dec, operating voltage below 1 V and low hysteresis are evidence of this. The gate-leakage is perhaps one of the drawbacks that can have the most effect on the end product as this usually results in power-hungry electronics. The long term stability (both bias stress and storage) of these CSorb devices are also much improved compared to our earlier semiconductor/insulator blend transistors.

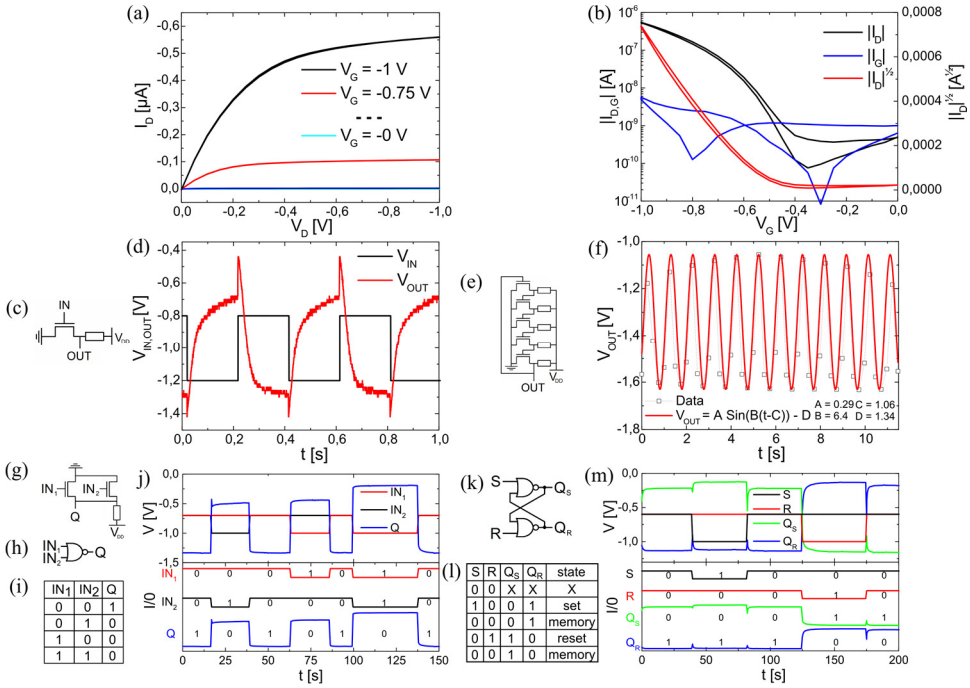


Figure 3.8. The solid CSorb transistor fabricated on paper was used to create all the devices represented in this figure; (a) Output- and (b) transfer characteristics, (c) inverter connection diagram and its (d) input and output, (e) ring-oscillator connection diagram and its (f) output, (g) and (h) NOR-gate connection diagram and its (i) truth table and (j) its inputs and outputs, (k) SR-latch connection diagram and its (l) truth table and (m) inputs and outputs.

The best performing solid CSorb blend paper transistor model was then used to build inverters with. The inverter setup can be seen in Figure 3.8 (c). The input and output curves of this inverter are plotted in Figure 3.8 (d). Important to observe here is that the output signal has larger amplitude than the inputs and, of course, that the signal is being inverted. Also, both the minimum and maximum of the input curve are within the minimum and maximum of the output curve. The switching speed of this inverter will eventually limit the speed of the end product. Therefore the faster this inverter switches, the faster electronics can be built. The speed of this environmentally friendly solid paper inverter is remarkably fast when compared to that of the inverters used in **Paper II**, when we take into account that there the state-of-the-art IL EMIM:TFSI was used and, further, that that device utilized an ICon in a liquid form. An ICon in solid state is almost always slower to reorganize its ions in an electric field compared to that in a liquid state, due to an increased internal resistance. A ring-oscillator was then built using the CSorb transistor. The device structure can be seen in Figure 3.8 (e) and its output in

Figure 3.8 (f). The propagation delay time per oscillation-stage of this device can then be compared to 35 ms of the fastest ring-oscillator presented in Section 3.2. Here we achieve 100 ms, which is only three times slower than the "environmentally dirty" liquid device.

We finally construct some actual electronic gates using these environmentally friendly transistors. The first gate to be constructed is the NOR-gate. This gate is constructed according to the scheme plotted in Figure 3.8 (g) using two CSorb paper transistors. The logic states that the device should follow are listed in the table in Figure 3.8 (i). The device has two inputs and one output that is false in all cases except if both inputs are in false states. A more detailed description of the NOR-gate can be found in Section 1.3.3. The output of this gate can be seen in Figure 3.8 (j). On top, the raw output is plotted, whereas in the bottom graph the curves are separated for clarity. The same basic requirements apply here as for the inverter; the output signal should be amplified compared to the input and no level-shifting should occur. The false state, for *this* gate, is defined as signals above -0.7 V and the true state below -1 V. One can see that the level of the false state, when only one of the two inputs is true, is different from that of the false state, when both inputs are true. This is partially due to the not-so-impressive on/off-ratio of the individual transistors, but also due to the fact that the driving potentials and resistance values have not been optimized. With optimization and mechanization of the fabrication processes even lower operating voltages could be utilized, resulting in less power hungry electronics as well, and as a result of, longer lasting electronics. The fact that the voltage levels are shifted from 0 V is not a problem per se, since a particular device built with these gates would all have the same true and false voltage-levels and when a separate device would be connected to this one, the output could be used as a positive or negative potential gradient as input for the next device, or other more sophisticated devices such as level-shifters or pull-up resistors could be used to shift the levels so that they would fit the levels of the next device. However, if the voltage-levels become too high, the individual transistors will start to degrade due to over oxidation and/or other electrochemical reactions occurring in the device. The reason for these voltage levels originates in the low transistor turn-on voltages. These could be improved by modifying the work functions of the source- drain- and especially the gate electrodes. This could be done by replacing the gold with e.g. carbon. Using carbon inks could also reduce the fabrication costs as well as simplify the fabrication processes when eventually transitioning to R2R-fabrication techniques.

The paper transistor is also used to create a one bit memory. This is achieved by building an SR-latch using four separate transistors. The SR-latch has two inputs and two outputs. The output can be in two separate distinct states.

Hence, these two states can be referred to as one true state and one false state. The two inputs are then used to control these output states. Only three distinct input states are allowed; the *SET*-state, the *RESET*-state and the *MEMORY (or READ)*-state. The two first states write a true- or false-state into the output and the *MEMORY*-state is used to read what state is stored in the memory. A more detailed description of the SR-latch can be found in Section 1.3.4. As long as there is a bias voltage applied, the memory is stored. Removing all other inputs will not affect the state of the one bit memory. The different distinct inputs and outputs can be seen in Figure 3.8 (l) and the actual device output can be seen in Figure 3.8 (m). It can be seen that the logic holds, as well as the fact that the same requirements on the amplification and voltage-levels, as was required of the earlier devices, also hold. Also, the output voltage holds after a state has been set, as long as the bias voltage is applied. This is one of the basic requirements of the one bit memory.

The logic gates presented above were manufactured using transistors that had been fabricated on samples containing only four transistors. The gates were then fabricated by connecting individual transistors and resistors with wires to complete the final electronic circuits. In order to demonstrate that these gates could also be fabricated in an R2R-compatible fashion, an integrated version of the SR-latch was developed. A schematic illustration of this has been plotted in Figure 3.9 (a) and (b) where the different device layers are separated and joined, respectively. A new method of applying the electrolyte was also needed, since spin casting is not compatible with R2R-fabrication techniques. The electrolyte was applied by means of doctor blading, using a piece of paper to spread out the solution. A picture of a finished SR-latch and a batch of four latches can be seen in Figure 3.9 (c) and (d), respectively. The output of the latch has been plotted in Figure 3.9 (e). Even though the electrolyte film deposition was un-even (non-optimized), as can be seen in Figure 3.9 (d), the output of the device was no worse than the previous latches created using individual transistors with spin casted electrolytic layers. This illustrates that the electrolyte and the fabrication methods of these devices are robust and not sensitive to small variations in the fabrication process.

More complicated logic, e.g. shift registers, [65] are also being developed. In order to realize this, n-channel transistors on the same substrate are also needed. Solution-processable and air stable n-channel semiconductors have already been demonstrated, but the use of a rough, absorptive paper substrate creates problems when trying to deposit the thin semiconductor layer. Developing a SC/INS n-channel blend, similar to the P3HT:PLLA blend, could be a solution to this problem. The use of CMOS technology would improve the switching speeds

of the devices, reduce the number of devices needed and also reduce the total power consumption of the circuits. [118]

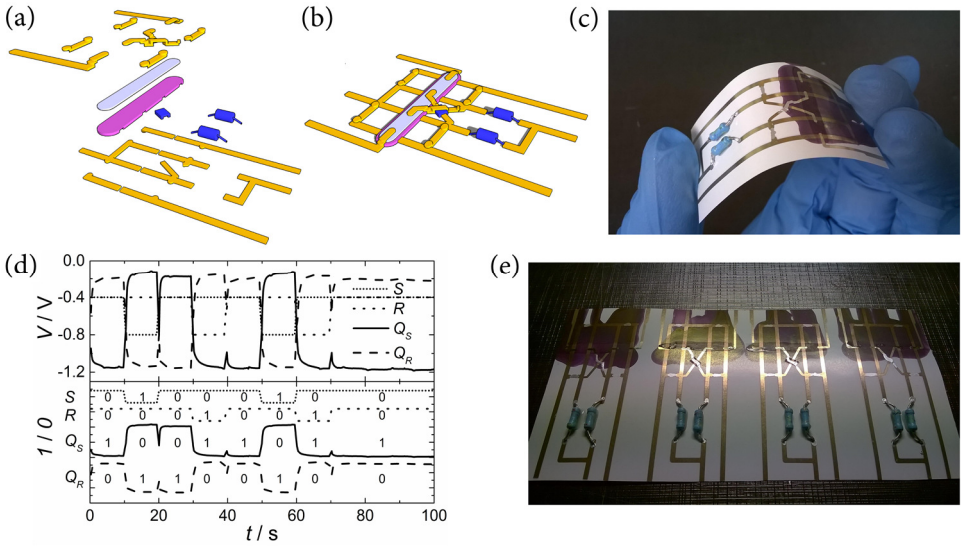


Figure 3.9. Graphical illustrations of the integrated SR-latch shown in (a) separate and (b) joined layers. (c) A picture of one SR-latch, (d) input- and output signals of the latch and a picture of four separate integrated SR-latches fabricated on one piece of paper.

3.4. Printed Environmentally Friendly Supercapacitors with Ionic Liquid Electrolytes on Paper

The performance and usefulness of the environmentally friendly electronics on paper presented so far in the previous sections, is a large leap from the membrane based electronics demonstrated in the beginning of the thesis. Nevertheless, all the devices presented so far, good or bad, are all operating at low-voltage, the main reasons being that the devices break down at higher voltages, low-voltage operation is less power-hungry, high-voltage shocks when handling the end products can be avoided, etc. Therefore, also a low-voltage power source on the same paper substrate is desirable. As the aim for the electronic components that are being built is recyclability and environmentally friendliness, the same requirements are then set on the power source as well. The materials and fabrication methods used should then also be environmentally friendly and cheap. Thus, the materials should be chosen so that they can be solution-processable at room temperature and that R2R-compatible fabrication techniques can be utilized. To that end, the most suitable device that fits all the above-mentioned parameters

is the supercapacitor (SuC). The SuCs presented in this chapter are based on the results presented in **Paper IV**.

The SuC has two main components: the electrodes and the ICon. The electrodes should be constructed so that they are porous and have a large surface area per mass of electrode material. The reason for this is that the capacitance of the capacitor is directly proportional to the surface area of the electrodes. One of the most commonly used electrode material in SuCs is AC. Surface areas of 1500 m^2/g are readily available using commercially available AC inks. [119] Depending on the binding material used for the AC and the size of the ions in the ICon, a wide range of effective surface area for the finished electrode, in the capacitor, can then be achieved. This, in turn, sets demands on the ICon used. It should carry a large enough charge, so that large capacitances can be achieved, but at the same time the physical size of the ions cannot exceed the sizes of the pores in the AC electrodes. One should also be aware that in an IL the positive and negative ions can form different kinds of layered structures. For instance, one positive charge can be surrounded by many negative ones, resulting in much larger charged "ion complexes" than what is perhaps intuitively expected. This can then result in a large portion of the smaller pore sizes in the AC electrodes never being utilized when the capacitor is being used. [71] The ICons that were used for the SuC were chosen on a similar basis as in the environmentally friendly transistors presented in Section 3.3, and as a result most of them are exactly the same. They are EcoEng, Reline, Glyceline and CSorb. The state-of-the-art IL EMIM:TFSI, used in Section 3.2, and Oxaline was also added to the ICons being investigated. The ICons used are all ionic only, with no solvent present, and the charges should be stored non-Faradaically on the electrodes during operation. The structure of the SuCs can be seen in Figure 3.10. The electrodes are printed on an aluminum coated paper using a pilot scale rotary screen printer. The ICons are printed using a laboratory scale screen printer and a cellulose paper is used as separator when two electrodes are laminated together. Different electrode sizes and substrates are presented in **Paper IV**, but the final "commercial" SuC setup printed on paper had a total thickness of 0.6 – 0.7 mm and an area of 56 cm^2.

The SuCs were investigated using impedance spectroscopy (IS) and cyclic charge discharge (CCD), in order to clarify their power storage capabilities and cycling stabilities. A Nyqvist diagram shown in Figure 3.11 (a) shows that the different ICons investigated have very different internal resistances. This is typically indicated by the real impedance ($\propto$ internal resistance) plotted on the x-axis. High internal resistances indicate that the EDLs at the electrode surfaces are being formed slowly. They also indicate that high-power-density-devices will be difficult to fabricate using those ICons. It does not, however, exclude the possibility

of creating high-energy-density-devices, as long as the capacitances are high enough. CCD measurements on the devices are perhaps more indicative of the actual power storage capabilities of the SuCs, as these measurements more resemble the type of situation the power supplies will be used in, in a real world application. The SuCs are charged and discharged at a constant current, repeatedly, and the power- and energy densities of the devices are then calculated. The results are plotted in a Ragone plot in Figure 3.11 (b).

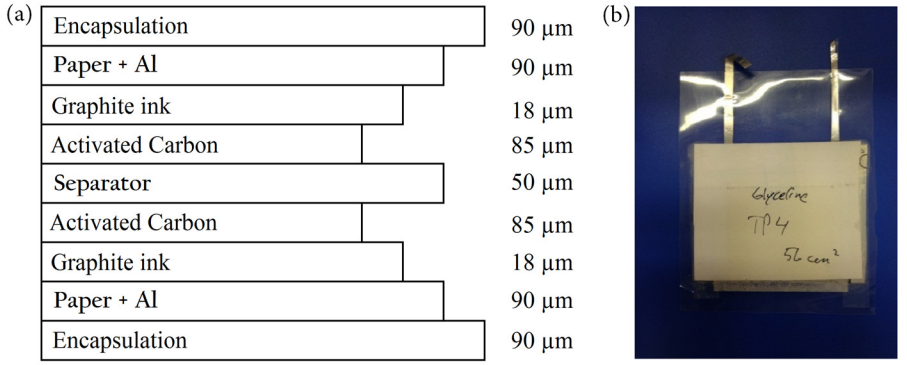


Figure 3.10. (a) Internal structure of the laminated SuC devices and (b) a picture of a laminated 56 cm² "commercial" SuC.

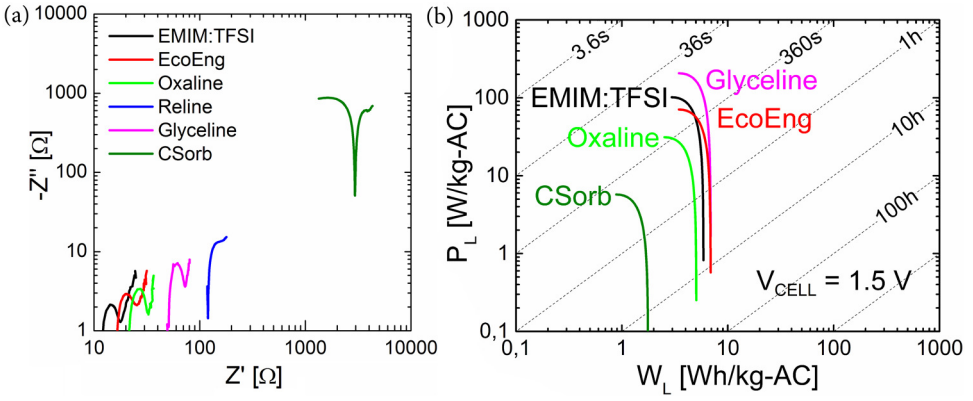


Figure 3.11. (a) A Nyqvist diagram and a (b) Ragone plot of the SuCs built using the different ICons. Z' and Z '' indicate real- and imaginary impedance, respectively, and P_L and W_L indicate power- and energy density, normalized according to the mass of AC used in the SuC, respectively.

It can be seen that Glyceline and the commercially available "green" alternative EcoEng have the highest energy densities, even higher than the state-of-the-art reference IL EMIM:TFSI, while the DEM Glyceline device has the highest power

density of all the devices fabricated. It is interesting that the CSorb SuC is so poor compared to the others, when it was clearly the best performer when used as ICon in the transistors presented in Section 3.3. One should, however, consider that these systems are quite different with smooth ICon/semiconductor interfaces in the transistor structure and rough ICon/electrode interfaces in the SuC structures. As a result, the wetting properties can be quite different in the two structures. The non-Faradaic power sources presented here are done using cheap fabrication methods and the materials used are also cheap and environmentally friendly. The SuCs built using the ChoCl based DEM Glyceline, outperform the commercially available state-of-the-art- and "green" IL alternative devices, both in power- and energy density.

The electronic circuits presented in this thesis, including the environmentally friendly supercapacitors, could all conceivably be fabricated on the same paper substrate and the step towards printing a whole electronic component in one go is closer to being realized. Other components needed, e.g. electrochromic displays and sensors, have already been demonstrated on PE-coated paper [120] and membrane [45] while other human interface components, e.g. capacitive touch sensors, [121] are still being developed. The devices presented here are of course in need of optimization, but the proof of concept has clearly been demonstrated.

4. Summary

A patterned self-supporting membrane is used in **Paper I** to combine two different types of low-voltage organic transistors in order to demonstrate that the membrane can be used as a platform for flexible electronics. The two transistor types presented complement each other (one operates in enhancement while the other operates in depletion) and more effective inverters can be built using both versions compared to using only one or the other. We demonstrate inverters and ring-oscillators using the different transistor types. Due to the nature of the membrane-based platform presented, the ion-conductor (ICon) is part of the membrane. While this device structure has several advantages, e.g. fewer fabrication steps, less electrochemistry with poly-electrolytic ICon and being environmentally benign, the switching speeds of the devices are critically low (on the order of seconds).

We therefore turned to other forms of ICons, namely ionic liquids. These have the advantage that high capacitances are achievable even at low-voltages and have been shown to switch much faster than e.g. poly-electrolytes. Since an ionic liquid is now used as ICon, the role of the membrane is no longer required. We therefore replace the membrane with another environmentally friendly, readily available and cheap alternative, namely paper. This substrate presented us with similar issues when applying the semiconductor, as the substrate is porous and absorptive. This, again, resulted in slow switching devices, but this time due to electrochemical doping of the semiconductor. We concluded that a thin semiconductor layer was needed on the paper substrate in order to speed up the devices.

The solution for creating a thin semiconductor layer on the absorptive substrate was to utilize a blend of semiconductor and insulator that was drop casted onto the substrate. During the drying process the semiconductor and insulator spontaneously phase-separated and created a layer of semiconductor on top of the insulator. During device operation the thin semiconductor layer could now be electrochemically doped and de-doped quickly during operation resulting in fast-switching devices. In **Paper II** we demonstrate how electronic components such as ring-oscillators can be fabricated to be up to 10 000 times faster using this technique of phase-separated semiconductor/insulator-blend compared to using the pure semiconductor.

In order to further improve the environmental aspect of the transistors, in **Paper III** the immidazolium-based ionic liquid is replaced by more environmentally benign and cheap alternatives, e.g. sorbitol- or urea-based ICons.

We demonstrate that these ICons can be used to create transistors on paper with comparable electronic properties as that of the state-of-the-art immidazolium-based ICon-transistors. Using a commercially available binder we solidify the ICon creating solid devices and use these to create inverters, ring-oscillators, NOR-gates and SR-latches or one bit memories. The R2R-compatibility of these devices is demonstrated further by creating an integrated-circuit-version of the memory device.

Finally, in **Paper IV** a fully printed flexible supercapacitor is fabricated on paper. The high-surface area, activated carbon electrodes are printed in a pilot scale trial and the same environmentally friendly ICons are used in these supercapacitors as in the transistors presented previously. The advantage of using these ICons is that higher operating voltages are achievable compared to that of other aqueous ICon alternatives where water hydrolysis becomes a problem at higher voltages. We also demonstrate that our supercapacitors can be cycled more than 10 000 times without showing degradation. This is due to the non-Faradaic nature of the energy storage mechanism that governs these devices. We also show that our devices have the same level of energy density as other commercially available supercapacitors, but at the same time show significantly lower power densities than those devices. Our "green" supercapacitors are, however, a cheap alternative to the commercially available state-of-the-art supercapacitors e.g. in applications where sharp power spikes are not required.

5. Conclusion and Outlook

The work presented in this thesis has advanced our knowledge of organic electronics, specifically the ion modulated transistor and the ionic liquid-based supercapacitor. The hygroscopic-insulator field-effect transistor had been developed and, further, the membrane-based transistor models as well as an aqueous electrolyte supercapacitor had been demonstrated at our university at the starting point of this thesis. The membrane based transistors were used to create complicated logic gates. The ionic liquid-based paper transistor was developed and using these devices, ring-oscillators were demonstrated. Both the ionic liquid and the semiconductor were then replaced with more environmentally friendly alternatives and complicated circuitry was demonstrated on paper using these devices. The supercapacitor development started with investigating different ionic liquids and ended up with environmentally friendly supercapacitors on paper being demonstrated. The fact that we use a paper substrate and environmentally friendly materials in our electronic devices, puts us at the forefront of our research field in the scientific community.

The next steps that naturally follows is creating CMOS on paper. This will entail developing an n-channel transistor on paper, e.g. by utilizing one of several commercially available, solution processable, n-type semiconductors. Similar problems, which were observed and solved in this thesis when creating p-channel devices on paper, are also expected for the envisioned n-channel devices. Perhaps similar solutions, i.e. using insulator/semiconductor blends, can be adopted here as well. A suitable cationic electrolyte to modulate the transistor channel must also be found. Using solution processable zinc oxide nano rods as semiconductor is also an alternative when creating n-channel transistors on paper.

All the steps involved in fabricating the different layers of the transistors and all the inter-connections between the different devices need to be applied by R2R-compatible processes. This is true for the paper devices presented in this thesis, in theory. However, entire devices are yet to be fabricated by one R2R-process. Once this is accomplished, more complicated circuitry, e.g. clocked flip-flops, can easily be realized. If we use the current, un-optimized, lifetime of these paper electronic devices as the restricting factor and assuming that the transistor fabrication process can be incorporated into the end-product manufacturing line, these transistors can be used in disposable electronic applications with short-term operational needs. These applications can be displays or indicators on food packages that warns the consumer if the food is spoiled or sensors on shipping crates providing location updates. If a different insulator that

does not spontaneously biodegrade is used in the blend, long term applications are also feasible. Applications such as humidity sensors in buildings, health monitor systems on the body or integrated into clothing as energy gathering are possible.

Apart from being used in most of the applications mentioned above, the energy storage units presented in this thesis, can also be used in countless other applications, especially if they are used in conjunction with conventional batteries. The main advantage with supercapacitors is that they can be cycled more times without degradation when compared to conventional rechargeable batteries. Therefore, supercapacitors can be used in low-voltage applications, e.g. toys, clocks and memories, as back-up power supplies for emergency doors or in transportation applications where repeated charging and discharging is needed.

The possibilities are endless when looking at possible applications for these cheap and disposable electronic circuits and energy storage units fabricated on a paper substrate.

Svensk resumé

Denna avhandling är baserad på fyra vetenskapliga artiklar, varav tre behandlar transistorer och komponenter byggda av transistorer och en behandlar superkondensatorer. Den organiska fälteffekttransistorn (OFETen) är modellkomponenten som har använts som utgångsläge för att tillverka transistorerna presenterade i denna avhandling. Man har dock ersatt isolatorn i OFETen med en jonledare (JL). Skillnaden mellan isolatorn och JLen är att den senare innehåller joner som är fysiskt mobila. Detta innebär att den jonmodulerade transistorn (JMTn) är potentialdriven istället för fälteffektdriven. Tjockleken på jonledaren i en potentialdriven transistor bestämmer inte hur mycket transistorn moduleras på samma sätt som i en fälteffektdriven transistor. Därför kan man enkelt tillverka lågspännings JMTn på ojämna underlag då man inte behöver kontrollera tjockleken på jonledaren.

Membranbaserade JMT versioner har utvecklats och använts för att tillverka en typ av kompletterande inverterare. Membranet innehåller både isolerande och jonledande delar och kan därför användas både som substrat för och JL i transistorerna. Vi demonstrerar membranens användbarhet som en flexibel plattform för elektronik genom att tillverka bl.a. en ring-oscillator som innehåller tio individuella transistorer. JLen i dessa transistorer är en poly-elektrolyt (med ena jonen immobil) vilket bl.a. gör att dessa transistorer är långsamma att byta läge. Vi övergick därför till en JL som har båda jonerna mobila och ersatte membranen med ett papperssubstrat. Detta resulterade i transistorer som hade större skillnad mellan av- och på-lägena, men det visade sig att dessa fortfarande var alltför långsamma.

Långsamheten berodde på den elektrokemi som sker när en transistor är i funktion. Det som tar tid är joner som rör sig in i halvledaren och dopar den. En tjockare halvledare tar längre tid att dopa. Vårt mål blev då att tillverka en tunn halvledare på ett poröst och absorberande papperssubstrat. Lösningen innefattade att blanda halvledaren med en isolator före dess applikation. Denna blandning droppades sedan på papperssubstratet och en spontan fasseparation skedde medan lösningsmedlet förångade bort. Resultatet blev ett tunt halvledarskikt på ett tjockt isolatorskikt. Miljövänligheten förbättrades också då isolatorn, som ersatt en stor del av den giftiga och dyra halvledaren, är billig och är komposterbar. När vi använde denna blandade halvledarversion kunde vi producera elektroniska komponenter som visade sig vara upp till 10 000 gånger snabbare.

Följande steg blev att byta ut JLen som innehåller giftiga fluorgrupper. Denna ersattes med en typ av miljövänliga djupa eutektiska blandningar (DEBar) som har liknande elektriska egenskaper som jonvätskor. Det visade sig att en DEB baserat på sorbitol hade de bästa elektriska egenskaperna. Denna var jämförbar med det bästa kommersiella alternativet, till och med när fasta transistorer tillverkats. Med hjälp av dessa transistorer demonstrerar vi inverterare, ring-oscillatorer, NOR-grindar och SR-grindar (en bits minne) på papper.

Slutligen bygger vi superkondensatorer med hjälp av dessa DEBar. En superkondensator är en plattkondensator med elektroder som har stor yta jämfört med dess volym och en JL emellan dessa elektroder. Våra superkondensatorer är tryckta på papper och elektroderna (aktiverat kol) är tryckta i en tryckmaskin på pilotskala medan JLna är schablontryckta på laboratorieskala. De 55 cm^2 stora och 700 μm tjocka superkondensatorerna, inklusive separator, är slutligen laminerade i plast. Jämfört med kommersiella alternativ innehåller våra superkondensatorer lika mycket energi- men mindre kraft per massa. Våra miljövänliga superkondensatorer är ändå ett trovärdigt alternativ som kan användas till ändamål där stora kraftspikar inte nödvändigtvis behövs.

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Paper- and Membrane-Based Ion-Modulated Electronics

The research on ion-modulated electronics reported in this doctoral thesis has been done at the physics department at the Faculty of Science and Engineering and within the Centre for Functional Materials at Åbo Akademi University.

The development of cheap and environmentally friendly electronics compatible with roll-to-toll printing techniques has been explored. Both organic and low-voltage transistors and supercapacitors have been fabricated on rough paper substrates using novel solution processing techniques.

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